Twin Builder Components: Power System VHDLAMS

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1 - Power System VHDL-AMS Library

The components in the Power System VHDL-AMS library are mostly first principle mathematical system-level models. The library has two main objectives:

- Provide reusable and extensible generic components for further customer design.
- Provide demonstrative application examples that use these types of components.

The Power System VHDL-AMS library consists of the following types of components:

- Basic
- Control Signal Generation
- Converter
- EMI EMC
- Transformer
- Transmission Line

Every component in the library has a related demonstrative example to show how the component works.

Basic

The Basic sub-library consists of basic components for power systems, it also includes fundamental components which are used in the other sub-libraries, and it contains:

- abc to alpha-beta-zero transformation
- alpha-beta-zero to abc transformation
- alpha-beta-zero to dq0 transformation
- dq0 to alpha-beta-zero transformation
- Ideal electromagnetic converter
- Magnetic reluctance
- Reluctance force actuator
- Ideal gyrator with no losses
- Ideal mutual inductor
- Lossless rotational electromechanical converter
- Lossless translational electromechanical converter
- Single phase ideal transformer
- AC current source (sinusoidal)
- Three phase AC current source (sinusoidal)
- Three phase sine wave generator
- Current controlled current source
- Voltage controlled current source
- Current controlled voltage source
- Voltage controlled voltage source
- Single phase circuit breaker
- Single phase switch
- Single phase two way switch

abc2abz : abc to alpha-beta-zero transformation

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

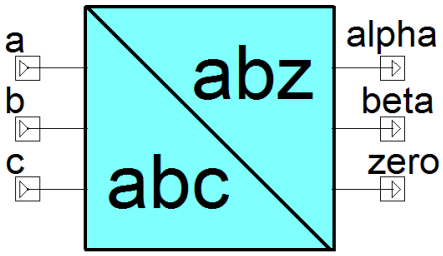

Figure 1. Component symbol

Description

The abc2abz model provides the calculation from a, b, c to alpha, beta, zero transform.

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$$\alpha = \frac{2}{3} \cdot a - \frac{1}{3} \cdot b - \frac{1}{3} \cdot c$$

$$\beta = \frac{1}{\sqrt{3}} \cdot b - \frac{1}{\sqrt{3}} \cdot c$$

$$zero = \frac{1}{3} \cdot a + \frac{1}{3} \cdot b + \frac{1}{3} \cdot c$$

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Input/Output Quantities

Table1

Name	Description [Unit]	Direction	Data Type
a	Input a.	Input	Real
b	Input b.	Input	Real
c	Input c.	Input	Real
alpha	Output alpha	Output	Real
beta	Output beta	Output	Real
zero	Output zero	Output	Real

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Transformations Example

abz2abc: alpha-beta-zero to abc transformation

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

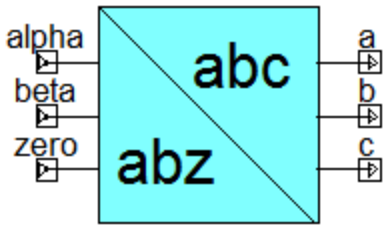

Figure 1. Component symbol

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Description

The abz2abc model provides the calculation from alpha, beta, zero to a, b, c transform.

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$$a = \alpha + zero$$

$$b = -\frac{1}{2} \cdot \alpha + \frac{\sqrt{3}}{2} \cdot \beta + zero$$

$$c = -\frac{1}{2} \cdot \alpha - \frac{\sqrt{3}}{2} \cdot \beta + zero$$

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Input/Output Quantities

Table1

Name	Description [Unit]	Direction	Data Type
alpha	Input alpha	Input	Real
beta	Input beta	Input	Real

zero	Input zero	Input	Real
a	Output a.	Output	Real
b	Output b.	Output	Real
c	Output c.	Output	Real

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Transformations Example

Load Transformation Example

abz2dq0 : alpha-beta-zero to dq0 transformation

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

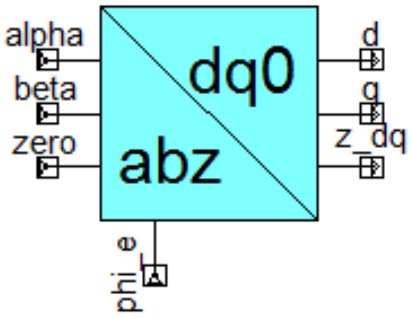

Figure 1. Component symbol

Description

The abz2dq0 provides the calculation from alpha, beta, zero to d, q, z_dq transform, with corresponding electrical angle from the motor.

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$$d = \alpha \cdot \cos(\phi_e) + \beta \cdot \sin(\phi_e)$$

$$q = -\alpha \cdot \sin(\phi_e) + \beta \cdot \cos(\phi_e)$$

$$z\_dq = zero$$

Netlist Syntax

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Input/Output Quantities

Table1

Name	Description [Unit]	Direction	Data Type
alpha	Input alpha.	Input	Real
beta	Input beta.	Input	Real
zero	Input zero.	Input	Real
phi_e	Input phi_e		
d	Output d	Output	Real
q	Output q	Output	Real
z_dq	Output z_dq	Output	Real

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Example

Transformations Example

circuit_breaker : Single phase circuit breaker

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

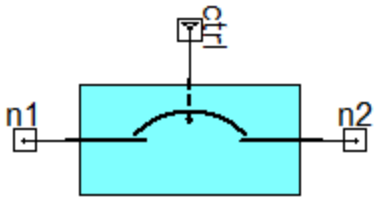

Figure 1. Component symbol

Description

The **circuit_breaker** represents a single phase circuit breaker with an external control signal to connect port 1 to port 2 with different resistance to represent close or open behavior.

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$$sw\_on <= ctrl'above(threshold)$$

$$\begin{cases} v = i \cdot R_{close} & sw\_on \ and \ ctrl >= threshold \\ v = i \cdot R_{open} & otherwise \end{cases}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
n1	Electrical port n1	electrical
n2	Electrical port n2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
R_close	Switch on resistance	resistance	1.0e-3 [Ohm]
R_open	Switch off resistance	resistance	1.0e6 [Ohm]
threshold	Threshold value	real	0.0

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
ctrl	Control signal input.	Input	Real

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Example

Switches Example

dq02abz : dq0 to alpha-beta-zero transformation

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

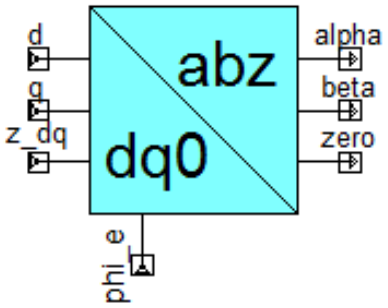

Figure 1. Component symbol

Description

The dq02abz provides the calculation from d, q, z_dq to alpha, beta, zero transform, with corresponding electrical angle from the motor.

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$$\alpha = d \cdot \cos(\phi_e) - q \cdot \sin(\phi_e)$$

$$\beta = d \cdot \sin(\phi_e) + q \cdot \cos(\phi_e)$$

$$zero = z\_dq$$

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Input/Output Quantities

Table1

Name	Description [Unit]	Direction	Data Type
d	Input d.	Input	Real
q	Input q.	Input	Real
Z_dq	Input z_dq.	Input	Real
phi_e	Input phi_e		
alpha	Output alpha	Output	Real
beta	Output beta	Output	Real
zero	Output zero	Output	Real

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Transformations Example

em_converter: Ideal electromagnetic converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

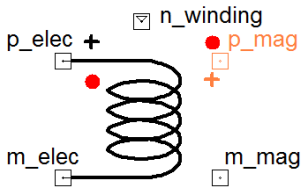

Figure 1. Component symbol

Description

The **em_converter** represents the behavior of an ideal electromagnetic converter, with a user defined number of winding turns.

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$$mmf = n_{winding} \cdot i$$

$$\begin{cases} flux = flux_0 & initial\ \ state \\ v = -n_{winding} \cdot \dfrac{d(flux)}{dt} & otherwise \end{cases}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_elec	Electrical port p_elec	electrical
m_elec	Electrical port m_elec	electrical
p_mag	Magnetic port p_mag	magnetic
m_mag	Magnetic port m_mag	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
n_wind-ing	Number of winding turns.	Input	Real

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Example

Simple ElectroMagnetic Example

gyrator: Ideal gyrator with no losses

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

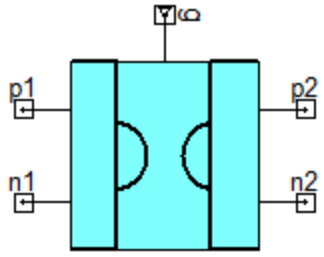

Figure 1. Component symbol

Description

The **gyrator** represents the behavior of an ideal gyrator with no losses.

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$$i_1 = g \cdot v_2$$

$$i_2 = -g \cdot v_1$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	magnetic
n_2	Electrical port n_2	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
g	Gyration conductance [A/V].	Input	Real

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Gyrator Example

i_ac: Single phase AC sinusoidal current source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

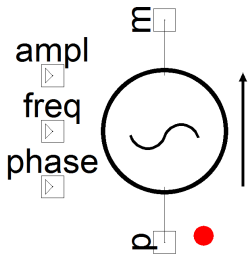

Figure 1. Component symbol

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- Mathematical Description

Description

The **i_ac** represents single phase ac sinusoidal current source.

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$$i = -ampl \cdot \sin 2\pi \cdot \left(freq \cdot time + \frac{phase}{360^o} \right)$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
m	Electrical port m	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ampl	Source amplitude [A]	Input	Real
freq	Source frequency [Hz]	Input	Real
phase	phase shift [degree]	Input	Real

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AC Sources Example

i_ac_3phase: Three phase AC sinusoidal current source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

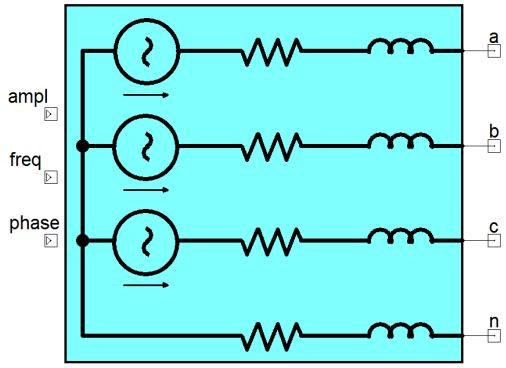

Figure 1. Component symbol

Description

The **i_ac_3phase** represents the behavior of 3 phase ac current source with symmetrical internal R-L impedances, the three current sources are connected in Y to neutral connection to external terminal.

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Table 1

Name	Port/Terminal description	Nature/Data type
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	magnetic
n	Electrical port n	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
r_l	line resistance	real	0.1 [Ohm]
l_l	line inductance	real	0.0001 [H]
r_n	resistance to neutral	real	0.1 [Ohm]
l_n	inductance to neutral	real	0.0001 [H]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
ampl	Source amplitude [A].	Input	Real
freq	Source frequency [Hz]	Input	Real
phase	Phase shift for Phase A [degree]	Input	Real

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Example

AC Sources Example

i_cc: Current controlled current source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

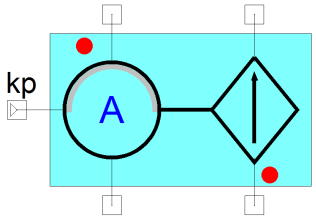

Figure 1. Component symbol

Description

The **i_cc** represents a current controlled current source.

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$$i_{source} = k \cdot i_{measure}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_am	Electrical port p_am.	electrical
m_am	Electrical port m_am	electrical
p_s	Electrical port p_s	electrical
m_s	Electrical port m_s	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
ts	sample time	real	0.0 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
kp	Current gain.	Input	Real

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Example

Controlled Sources Example

i_vc: Voltage controlled current source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

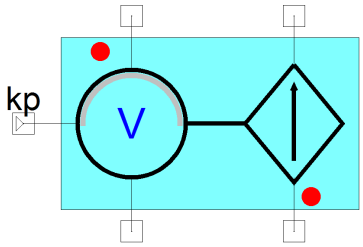

Figure 1. Component symbol

Description

The **i_vc** represents a voltage controlled current source.

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$$i_{source} = k \cdot v_{measure}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_am	Electrical port p_am.	electrical
m_am	Electrical port m_am	electrical
p_s	Electrical port p_s	electrical
m_s	Electrical port m_s	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
ts	sample time	real	0.0 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
kp	Current gain.	Input	Real

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Example

Controlled Sources Example

inductor_mutual: Ideal mutual inductor

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

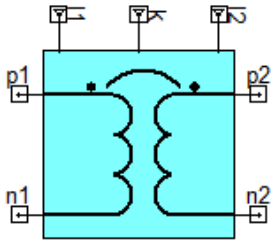

Figure 1. Component symbol

Description

The **inductor_mutual** represents the behavior of an ideal mutual inductor with no losses.

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$$v_1 = L_1 \cdot \frac{di_1}{dt} + M \frac{di_2}{dt}$$

$$v_2 = L_2 \cdot \frac{di_2}{dt} + M \frac{di_1}{dt}$$

$$M = k \cdot \sqrt{L_1 \cdot L_2}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
i1_0	initial current for L1	current	0.0 [A]
i2_0	initial current for L2	current	0.0 [A]
use_i0	use initial currents or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
k	Coefficient of coupling. 0<k<1	Input	Real
l1	self inductance for inductor 1	Input	Inductance
l2	self inductance for inductor 2	Input	Inductance

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Mutual Inductor Example

reluctance: Magnetic reluctance

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

Description

The **reluctance** represents the behavior of a magnetic reluctance. The reluctance value depends on the geometry of the modeled section.

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$$\mu_0 = 4\pi \cdot 10^{-7} \ [H/m]$$

$$r = \frac{g}{\mu_0 \cdot \mu_r \cdot A}$$

$$mmf = r \cdot flux$$

where μ_0 is the permeability constant, the amount of resistance encountered when forming a magnetic field in a classical vacuum. r is the reluctance.

Netlist Syntax

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Table 1

Name	Port/Terminal description	Nature/Data type
p_mag	Magnetic port p_mag	magnetic
m_mag	Magnetic port m_mag	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
A	Cross sectional area.	Real	0.01 [m^2]
mu_r	Relative permeability of material	Real	1.0

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
g	Thickness or length of section or gap [m]	Input	Real

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Example

Simple ElectroMagnetic Example

remc: Lossless rotational electromechanical converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

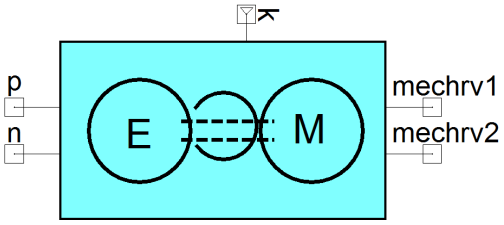

Figure 1. Component symbol

Description

The **remc** represents the behavior of lossless rotational electromechanical converter, based on a user defined quantity k.

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Mathematical Description

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$$v = k \cdot omega$$

$$tau = -k \cdot i$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
mechrv1	Mechanical port mechrv1	rotational_velocity
mechrv2	Mechanical port mechrv2	rotational_velocity

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
k	Coefficient of trans-formation [V/(rad/s)]	Input	Real

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Example

Rotational Electromechanical Converter Example

rfa: Reluctance force actuator

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

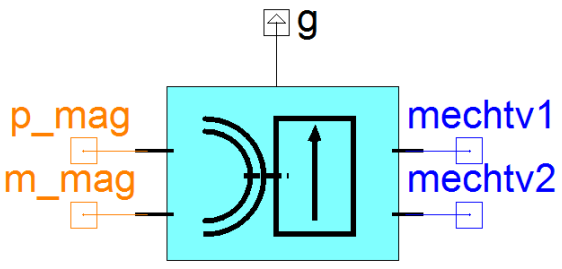

Figure 1. Component symbol

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- Assumptions and Limitations

Description

The **rfa** represents the behavior of reluctance force actuator.

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Assumptions and Limitations

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Mathematical Description

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$$\mu_0 = 4\pi \cdot 10^{-7}\ [H/m]$$

$$\begin{cases} g = g_0 & initial\ \ state \\ u = \dfrac{dg}{dt} & otherwise \end{cases}$$

$$\begin{cases} r = \dfrac{g}{\mu_0 \mu_r A} & g > g_{\min} \\ r = \dfrac{g_{\min}}{\mu_0 \mu_r A} & otherwise \end{cases}$$

$$\begin{cases} f = -\dfrac{flux^2}{2\mu_0 \mu_r A} & g > g_{\min} \\ f = -\dfrac{flux^2}{2\left(\mu_0 \mu_r A + c_{stiff}\left(g_{\min} - g\right) - c_{damp} u\right)} & otherwise \end{cases}$$

$$mmf = flux \cdot r$$

where μ_0 is the permeability constant, the amount of resistance encountered when forming a magnetic field in a classical vacuum. r is the reluctance. u is the mechanical side move velocity.

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Table 1

Name	Port/Terminal description	Nature/Data type
p_mag	Magnetic port p_mag	magnetic
m_mag	Magnetic port m_mag	magnetic
mechtv1	Mechanical port mechtv1	translational_velocity
mechtv2	Mechanical port mechtv2	translational_velocity

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
g0	Initial air gap	real	0.002 [m]
gmin	Minimum air gap	real	1.0e-7 [m]
A	Cross sectional area	real	0.01 [m^2]
mu_r	Relative permeability of material	real	1.0
c_stiff	Contact stiffness after hitting the gmin	real	1.0e6 [N/m]
c_damp	Contact damping after hitting the gmin	real	500.0 [N*s/m]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
g	Thickness or length of section or gap [m]	Output	Real

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Example

Simple ElectroMagnetic Example

sine_3phase: Three phase sine wave generator

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

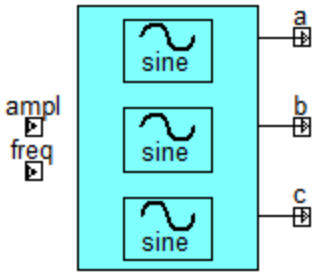

Figure 1. Component symbol

Description

The **sine_3phase** represents 3 phase sine waves.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
phase	Phase shift for Phase A	angle	0.0 [rad]
off	offset	real	0.0
tdelay	time delay	real	0.0 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
ampl	Source amplitude.	Input	Real
freq	Source frequency [Hz]	Input	Real

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Example

AC Sources Example

switch: Single phase switch

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

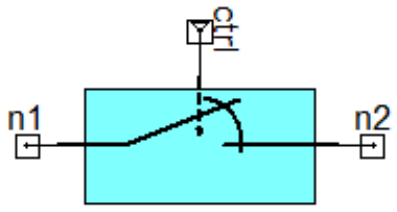

Figure 1. Component symbol

Description

The **switch** represents a single phase switch with an external control signal to connect port 1 to port 2 with different resistance to represent close or open behavior.

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$$sw\_on <= ctrl'above(threshold)$$

$$\begin{cases} v = i \cdot R_{close} & sw\_on \ and \ ctrl > threshold \\ v = i \cdot R_{open} & otherwise \end{cases}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
n1	Electrical port n1	electrical
n2	Electrical port n2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
R_close	Switch on resistance	resistance	1.0e-3 [Ohm]
R_open	Switch off resistance	resistance	1.0e6 [Ohm]
threshold	Threshold value	real	0.0

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
ctrl	Control signal input.	Input	Real

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Example

Switches Example

switch2 : Single phase two way switch

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

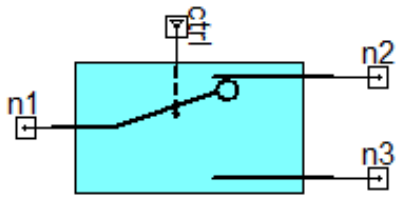

Figure 1. Component symbol

Description

The **switch2** represents a single phase two way switch with an external control signal to connect port 1 to port 2 or port 3 with different resistance.

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$$sw\_on <= ctrl'above(threshold)$$

$$\begin{cases} v_1 = i_1 \cdot R_{close} & sw\_on \ and \ ctrl >= threshold \\ v_1 = i_1 \cdot R_{open} & otherwise \end{cases}$$

$$\begin{cases} v_2 = i_2 \cdot R_{open} & sw\_on \ and \ ctrl >= threshold \\ v_2 = i_2 \cdot R_{close} & otherwise \end{cases}$$

Netlist Syntax

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Table 1

Name	Port/Terminal description	Nature/Data type
n1	Electrical port n1	electrical
n2	Electrical port n2	electrical
n3	Electrical port n3	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
R_close	Switch on resistance	resistance	1.0e-3 [Ohm]
R_open	Switch off resistance	resistance	1.0e6 [Ohm]
threshold	Threshold value	real	0.0

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
ctrl	Control signal input.	Input	Real

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Example

Switches Example

temc: Lossless translational electromechanical converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

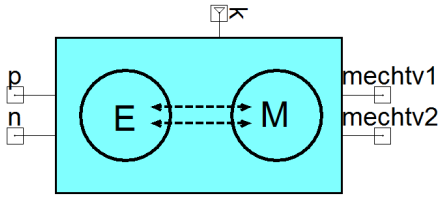

Figure 1. Component symbol

Description

The **temc** represents the behavior of lossless translational electromechanical converter, based on an user defined quantity k.

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$$v = k \cdot velocity$$

$$force = -k \cdot i$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
mechtv1	Mechanical port mechtv1	translational_velocity
mechtv2	Mechanical port mechtv2	translational_velocity

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
k	Coefficient of trans-formation [V/(rad/s)].	Input	Real

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Example

Translational Electromechanical Converter Example

transformer_ideal: Single phase ideal transformer

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

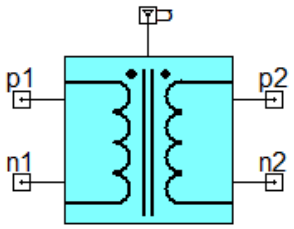

Figure 1. Component symbol

Description

The **transformer_ideal** represents the behavior of an ideal single phase transformer model with no losses and user defined number of winding turns.

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$$v_1 = n \cdot v_2$$

$$i_2 = -n \cdot i_1$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
n	Number of winding turns.	Input	Real

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Example

Ideal Transformer Example

v_cc: Current controlled voltage source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

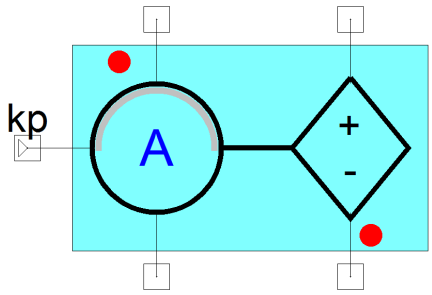

Figure 1. Component symbol

Description

The **v_cc** represents a current controlled voltage source.

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$$v_{source} = k \cdot i_{measure}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_am	Electrical port p_am.	electrical
m_am	Electrical port m_am	electrical
p_s	Electrical port p_s	electrical
m_s	Electrical port m_s	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
ts	sample time	real	0.0 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
kp	Current gain.	Input	Real

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Example

Controlled Sources Example

v_vc: Voltage controlled voltage source

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

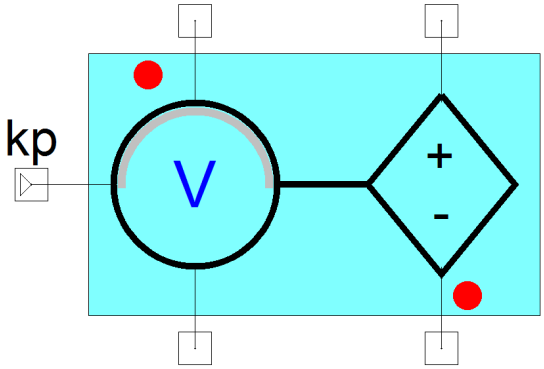

Figure 1. Component symbol

Description

The **v_vc** represents a voltage controlled voltage source.

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$$v_{source} = k \cdot v_{measure}$$

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Table 1

Name	Port/Terminal description	Nature/Data type
p_am	Electrical port p_am.	electrical
m_am	Electrical port m_am	electrical
p_s	Electrical port p_s	electrical
m_s	Electrical port m_s	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
ts	sample time	real	0.0 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
kp	Current gain.	Input	Real

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Controlled Sources Example

Control Signal Generation

The Control Signal Generation sub-library consists of 2-level, 3 level PWM signal generation components for power systems. The PWM generators can be directly used with the converter components in the Converter sublibrary, and it contains:

- Space vector PWM signal for 2 level three phase converter
- 2 level PWM generator for 2 pulse converter with internal reference
- 2 level PWM generator for 2 pulse converter with external reference
- 2 level PWM generator for 4 pulse converter with internal reference
- 2 level PWM generator for 4 pulse converter with external reference (bipolar)
- 2 level PWM generator for 4 pulse converter with external reference (unipolar)
- 2 level PWM generator for 6 pulse converter with internal reference
- 2 level PWM generator for 6 pulse converter with external reference
- 3 level PWM generator for 4 pulse converter with internal reference
- 3 level PWM generator for 4 pulse converter with external reference
- 3 level PWM generator for 8 pulse converter with internal reference
- 3 level PWM generator for 8 pulse converter with external reference
- 3 level PWM generator for 12 pulse converter with internal reference
- 3 level PWM generator for 12 pulse converter with external reference

pwm22e: 2 level 2 pulse PWM generator with external reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

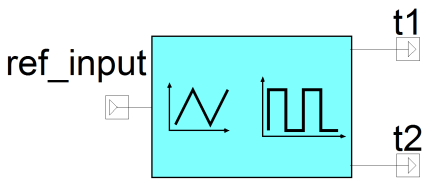

Figure 1. Component symbol

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Description

The **pwm22e** represents 2 level PWM generator for single phase 2 pulse (half-bridge) converter with external reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_input	external reference signal	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real

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Example

Two Level Two Pulse PWM Example

pwm22i: 2 level 2 pulse PWM generator with internal reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

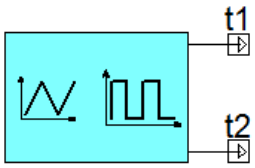

Figure 1. Component symbol

Description

The **pwm22i** represents 2 level PWM generator for single phase 2 pulse (half bridge) converter with internal sinusoidal reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real

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Example

Two Level Two Pulse PWM Example

pwm24eb: 2 level 4 pulse PWM with external reference, bipolar

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

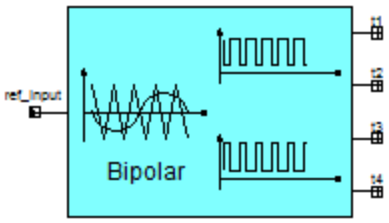

Figure 1. Component symbol

Description

The **pwm24eb** represents 2 level PWM generator for single phase 4 pulse (full-bridge) converter with external reference signal and natural sampling, in bipolar mode.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_input	external reference signal	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real

t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real

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Example

Two Level Four Pulse PWM Example

pwm24eu: 2 level 4 pulse PWM with external reference, unipolar

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

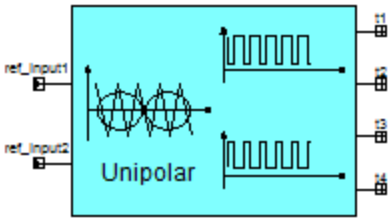

Figure 1. Component symbol

Description

The **pwm24eu** represents 2 level PWM generator for single phase 4 pulse (full-bridge) converter with external reference signal and natural sampling, in unipolar mode.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_input1	external reference signal 1	Input	Real
ref_input2	external reference signal 2	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real

t4	PWM signal for t4	Output	Real

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Example

Two Level Four Pulse PWM Example

pwm24i: 2 level 4 pulse PWM generator with internal reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

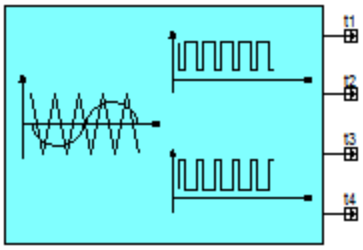

Figure 1. Component symbol

Description

The **pwm24i** represents 2 level PWM generator for single phase 4 pulse (full-bridge) converter with internal sinusoidal reference signal and natural sampling. It includes both unipolar and bipolar behaviors.

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TopNote: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real

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Two Level Four Pulse PWM Example

pwm26e: 2 level three phase PWM generator with external references

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

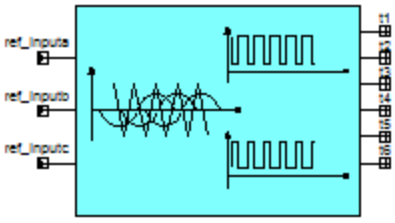

Figure 1. Component symbol

Description

The **pwm26e** represents the behavior of 2 level PWM generator for three phase 6 pulse converter with external reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_inputA	external reference signal A	Input	Real
ref_inputB	external reference signal B	Input	Real
ref_inputC	external reference signal C	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real

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Two Level Six Pulse PWM Example

pwm26i: 2 level three phase PWM generator with internal reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

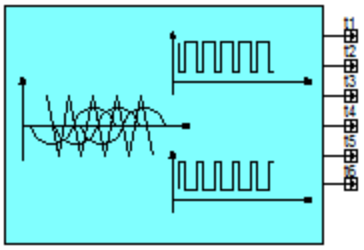

Figure 1. Component symbol

Description

The **pwm26i** represents the behavior of 2 level PWM generator for three phase 6 pulse converter with internal sinusoidal reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
min_car	Minimum value of the triangle carrier, the midpoints is calculated by (min+max)/2	real	-1.0
max_car	Maximum value of the triangle carrier, the midpoint is calculated by (min+max)/2	real	1.0
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
tdelay	Initial time delay of the triangle carrier, 0.0 means that the triangle signal initial position is set to midpoint between its minimum and maximum value and the slope is positive	real	0.0 [rad]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real

t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real

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Example

Two Level Six Pulse PWM Example

pwm34e: 3 level 4 pulse PWM generator with external reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

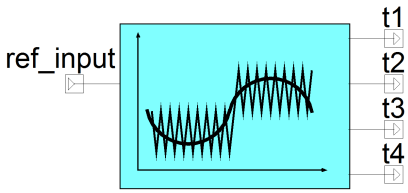

Figure 1. Component symbol

Description

The **pwm34e** represents 3 level PWM generator for single phase 4 pulse (half-bridge) converter with external reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_input	external reference signal	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real

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Example

Three Level Four Pulse PWM Example

pwm34i: 3 level 4 pulse PWM generator with internal reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

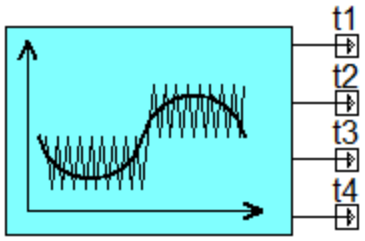

Figure 1. Component symbol

Description

The **pwm34i** represents 3 level PWM generator for single phase 4 pulse (half-bridge) converter with internal sinusoidal reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100.0 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real

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Example

Three Level Four Pulse PWM Example

pwm38e: 3 level 8 pulse PWM generator with external reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

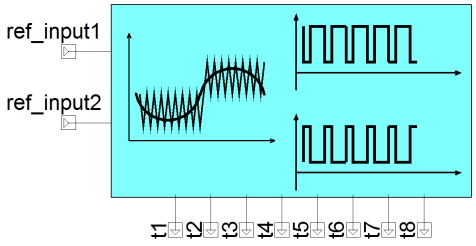

Figure 1. Component symbol

Description

The **pwm38e** represents 3 level PWM generator for single phase 8 pulse (full-bridge) converter with external reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_ time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_ input1	external reference signal 1	Input	Real
ref_ input2	external reference signal 2	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real
t7	PWM signal for t7	Output	Real
t8	PWM signal for t8	Output	Real

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Example

Three Level Eight Pulse PWM Example

pwm38i: 3 level 8 pulse PWM generator with internal reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

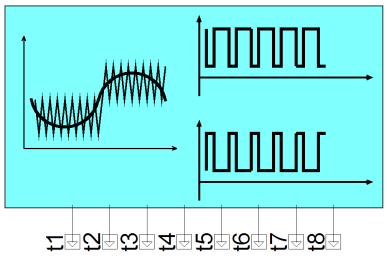

Figure 1. Component symbol

Description

The **pwm38i** represents 3 level PWM generator for single phase 8 pulse (full-bridge) converter with internal reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100.0 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real
t7	PWM signal for t7	Output	Real
t8	PWM signal for t8	Output	Real

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Example

Three Level Eight Pulse PWM Example

pwm312e: 3 level 12 pulse PWM generator with external reference

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

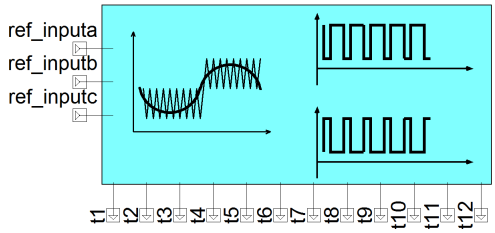

Figure 1. Component symbol

Description

The **pwm312e** represents 3 level PWM generator for three phase 12 pulse converter with external reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_ time	dead time of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
ref_ inputA	external reference signal A	Input	Real
ref_ inputB	external reference signal B	Input	Real
ref_ inputC	external reference signal C	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real
t7	PWM signal for t7	Output	Real
t8	PWM signal for t8	Output	Real
t9	PWM signal for t9	Output	Real
t10	PWM signal for t10	Output	Real
t11	PWM signal for t11	Output	Real
t12	PWM signal for t12	Output	Real

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Three Level Twelve Pulse PWM Example

pwm312i: 3 level 12 pulse PWM generator with internal reference

Library: Power System	Modeling Language:	Version Number: Twin

VHDLAMS	VHDL-AMS	Builder 2024.2

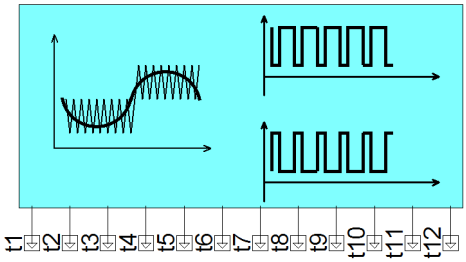

Figure 1. Component symbol

Description

The **pwm312i** represents 3 level PWM generator for three phase 12 pulse converter with internal reference signal and natural sampling.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 1

Name	Description	Data Type	Default Value [Unit]
freq	switching frequency of the triangle carrier	real	1000.0 [Hz]
dead_time	dead time of switching	real	100.0e-9 [sec]
modu_ind_ref	modulation index of the reference signal, it should be in the range of (0,1].	real	0.8
freq_ref	switching frequency of the reference signal	real	100.0 [Hz]
phase_ref	phase shift of the reference signal	real	0.0 [rad]

Input/Output Quantities

Table 2

Name	Description [Unit]	Direction	Data Type
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real
t7	PWM signal for t7	Output	Real
t8	PWM signal for t8	Output	Real
t9	PWM signal for t9	Output	Real
t10	PWM signal for t10	Output	Real
t11	PWM signal for t11	Output	Real
t12	PWM signal for t12	Output	Real

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Three Level Twelve Pulse PWM Example

svpwm: Space vector PWM signal generator

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

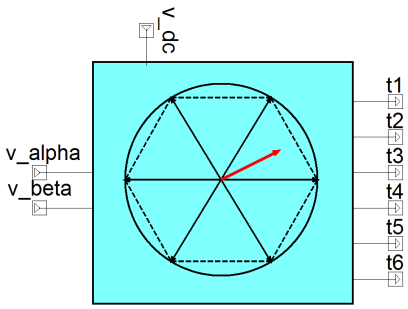

Figure 1. Component symbol

Description

The **svpwm** represents the behavior of space vector PWM generator for 2 level three phase converters.

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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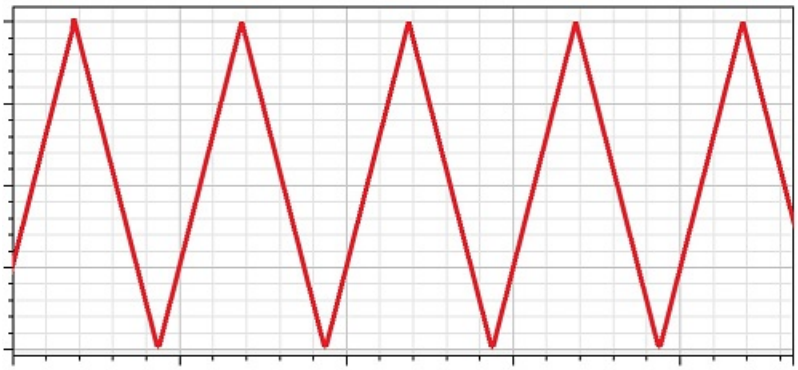
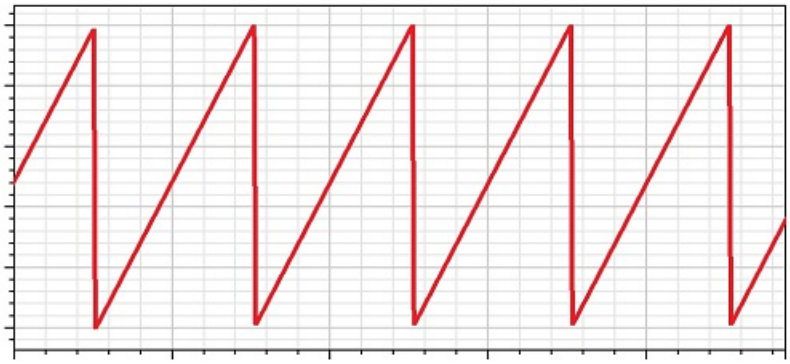
Use the **Simulator Model** drop-down menu to select the carrier wave option used in the **svpwm** generator.

- **mid_align** – Use the triangle source for the carrier wave.



- **right_align** – Use the right sawtooth source for the carrier wave.



- **left_align** – Use the left sawtooth source for the carrier wave.

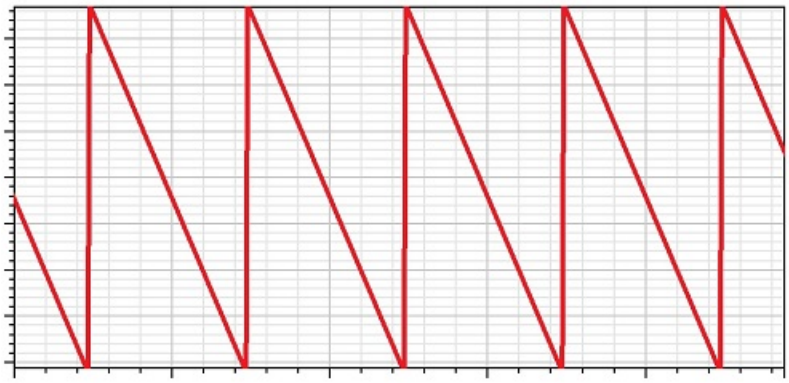


Table 1

Name	Description	Data Type	Default Value [Unit]
freq	Switching frequency	real	1000.0 [Hz]
dead_time	Deadtime of switching	real	100.0e-9 [sec]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
v_dc	DC voltage signal [V]	Input	Real
v_alpha	Reference v_alpha signal [V]	Input	Real
v_beta	Reference v_beta signal [V]	Input	Real
t1	PWM signal for t1	Output	Real
t2	PWM signal for t2	Output	Real
t3	PWM signal for t3	Output	Real
t4	PWM signal for t4	Output	Real
t5	PWM signal for t5	Output	Real
t6	PWM signal for t6	Output	Real

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SVPWM Example

Converter

The Converter sublibrary consists of 2-level, 3 level converter components for power systems. All the converter models can be used as either rectifier or inverter. The converters can be directly used with the PWM generator models in the Control Signal Generation sub-library, and it contains:

- 2 level half bridge resonance converter
- 2 level full bridge resonance converter
- 2 level three phase resonance converter
- 3 level half bridge resonance converter
- 3 level full bridge resonance converter
- 3 level three phase resonance converter
- Single phase to single phase cycloconverter
- Single phase to single phase cycloconverter with sinusoidal variation of firing angle
- Three phase to single phase half wave cycloconverter
- Three phase to three phase half wave cycloconverter
- Matrix converter with SVPWM control
- Matrix converter with Venturini control
- Three phase T-Type inverter
- Vienna rectifier

tprc: three phase resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

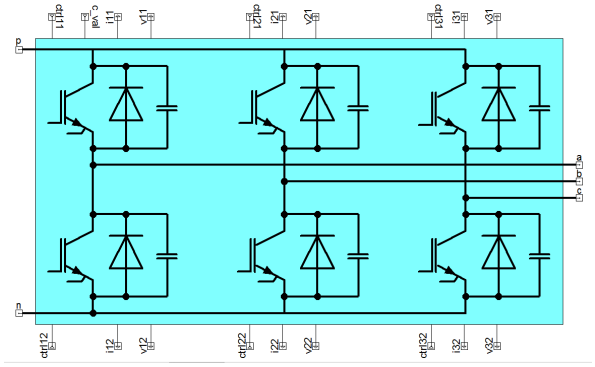

Figure 1. Component symbol

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Description

The tprc represents the behavior of a three phase resonant converter.

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value	Input	capacitance
ctrl11	control input signal 11	Input	real
ctrl12	control input signal 12	input	real
ctrl21	control input signal 21	Input	real
ctrl22	control input signal 22	input	real
ctrl31	control input signal 31	Input	real

ctrl32	control input signal 32	input	real
i11	current measurement at phase A upper side	output	current
v11	voltage measurement at phase A upper side	output	voltage
i12	current measurement at phase A lower side	output	current
v12	voltage measurement at phase A lower side	output	voltage
i21	current measurement at phase B upper side	output	current
v21	voltage measurement at phase B upper side	output	voltage
i22	current measurement at phase B lower side	output	current
v22	voltage measurement at phase B lower side	output	voltage
i31	current measurement at phase C upper side	output	current
v31	voltage measurement at phase C upper side	output	voltage
i32	current measurement at phase C lower side	output	current
v32	voltage measurement at phase C lower side	output	voltage

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Three Phase Resonant Converter Example

tprc3: 3 level three phase resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

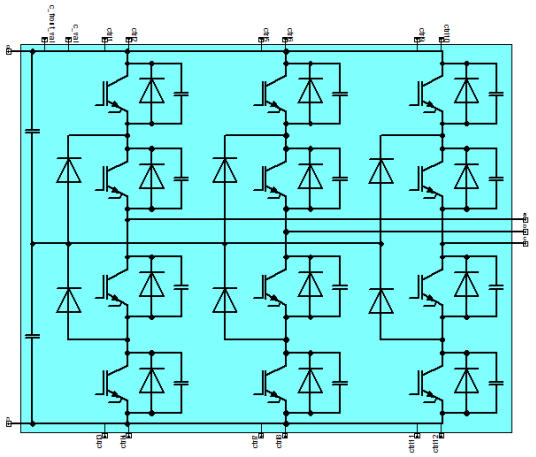

Figure 1. Component symbol

Description

The **tprc3** represents the behavior of a three level three phase resonant converter.

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_front_v0	front capacitance initial voltage	voltage	0.0 [V]

c_use_front_v0	use initial voltage or not for front capacitance	Boolean	false
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value.	Input	capacitance
c_front_val	front capacitance value.	Input	capacitance
ctrl1	control input signal 1	Input	real
ctrl2	control input signal 2	input	real
ctrl3	control input signal 3	Input	real
ctrl4	control input signal 4	input	real
ctrl5	control input signal 5	Input	real
ctrl6	control input signal 6	input	real
ctrl7	control input signal 7	Input	real
ctrl8	control input signal 8	input	real
ctrl9	control input signal 9	Input	real
ctrl10	control input signal 10	input	real
ctrl11	control input signal 11	Input	real
ctrl12	control input signal 12	input	real

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Three Level Three Phase Resonant Converter Example

fbrc: Full bridge resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

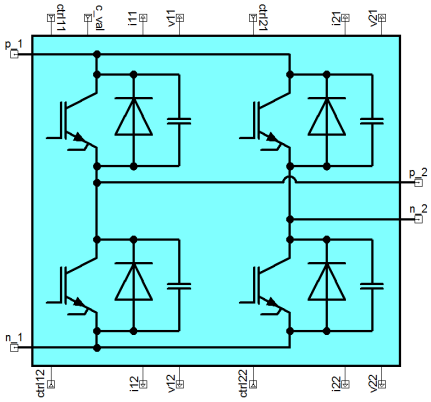

Figure 1. Component symbol

Description

The **fbrc** represents the behavior of a single phase full bridge resonant converter.

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value.	Input	capacitance
ctrl11	control input signal 11	Input	real
ctrl12	control input signal 12	input	real
ctrl21	control input signal 21	input	real
ctrl22	control input signal 22	input	real
i11	current measurement at first phase leg upper side	output	current
v11	voltage measurement at first phase leg upper side	output	voltage
i12	current measurement at first phase leg lower side	output	current
v12	voltage measurement at first phase leg lower side	output	voltage
i21	current measurement at second phase leg upper side	output	current
v21	voltage measurement at second phase leg upper side	output	voltage
i22	current measurement at second phase leg lower side	output	current
v22	voltage measurement at second phase leg lower side	output	voltage

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Full Bridge Resonant Converter Example

fbrc3: 3 level full bridge resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

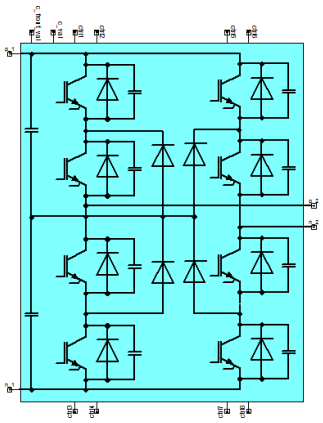

Figure 1. Component symbol

Description

The **fbrc3** represents the behavior of a single phase 3 level full bridge resonant converter.

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_front_v0	front capacitance initial voltage	voltage	0.0 [V]
c_use_front_v0	use initial voltage or not for the front capacitance	Boolean	false
c_v0	capacitance initial voltage	voltage	0.0 [V]

c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value.	Input	capacitance
c_front_val	front capacitance value	Input	capacitance
ctrl1	control input signal 1	Input	real
ctrl2	control input signal 2	input	real
ctrl3	control input signal 3	Input	real
ctrl4	control input signal 4	input	real
ctrl5	control input signal 5	Input	real
ctrl6	control input signal 6	input	real
ctrl7	control input signal 7	Input	real
ctrl8	control input signal 8	input	real

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Example

Three Level Full Bridge Resonant Converter Example

hbrc: Half bridge resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

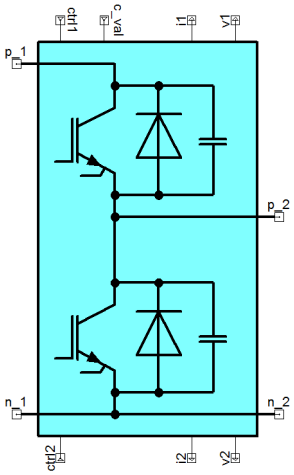

Figure 1. Component symbol

Description

The **hbrc** represents the behavior of a single phase half bridge resonant converter.

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value.	Input	capacitance
ctrl1	control input signal 1	Input	real
ctrl2	control input signal 2	input	real
i1	current measurement at upper side	output	current
v1	voltage measurement at upper side	output	voltage
i2	current measurement at lower side	output	current
v2	voltage measurement at lower side	output	voltage

Top

Example

Half Bridge Resonant Converter Example

hbrc3: 3 level half bridge resonance converter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

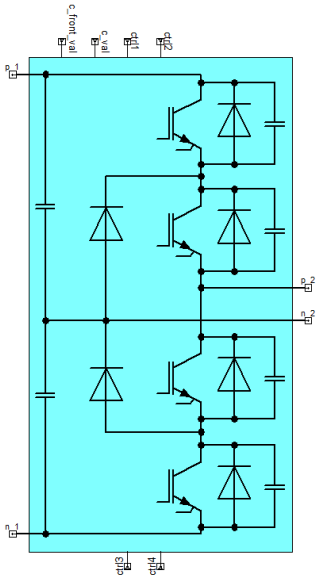

Figure 1. Component symbol

Description

The **hbrc3** represents the behavior of a 3 level single phase half bridge resonant converter.

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Assumptions and Limitations

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Table 1

Name	Port/Terminal description	Nature/Data type
p_1	Electrical port p_1	electrical
n_1	Electrical port n_1	electrical
p_2	Electrical port p_2	electrical
n_2	Electrical port n_2	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_front_v0	front capacitance initial voltage	voltage	0.0 [V]
c_use_front_v0	use initial voltage for front capacitance or not	Boolean	false
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance voltage or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value.	Input	capacitance
c_front_val	front capacitance value	Input	capacitance
ctrl1	control input signal 1	Input	real
ctrl2	control input signal 2	input	real

ctrl3	control input signal 3	input	real
ctrl4	control input signal 4	input	real

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Example

Three Level Half Bridge Resonant Converter Example

cyclo1_1: Single-phase to single-phase cycloconverter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

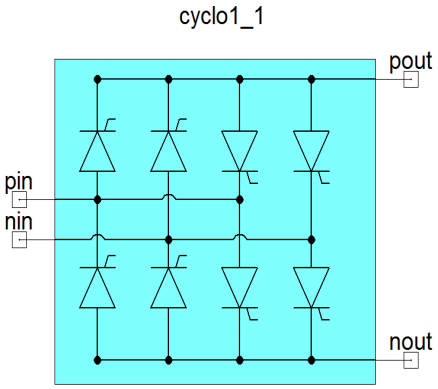

Figure 1. Component symbol

Description

The **cyclo1_1** represents the behavior of a single-phase to single-phase cycloconverter. The component reduces the frequency of the input voltage and will also reduce the RMS value of the output.

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Assumptions and Limitations

Top

Output frequency is less than that of the input frequency.

Alpha must be between 0-179.5 degrees.

Divisor must be an integer greater than zero.

Mathematical Description

Top

$$Divisor = frequency_{input} / frequency_{output}$$

Netlist Syntax

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Conservative Pins

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Table 1

Name	Port/Terminal description	Nature/Data type
pin	Electrical port pin	electrical
nin	Electrical port nin	electrical
pout	Electrical port pout	electrical
nout	Electrical port nout	electrical

Parameters

Top

Table 2

Name	Description	Data Type	Default Value [Unit]
freq_in	input voltage frequency	real	60.0 [Hz]
divisor	frequency conversion divisor	real	2.0

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
alpha	firing angle [Degrees]	Input	real

Top

Example

cyclo1_1sin: Single-phase to single-phase cycloconverter with sinusoidal variation of firing angle

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

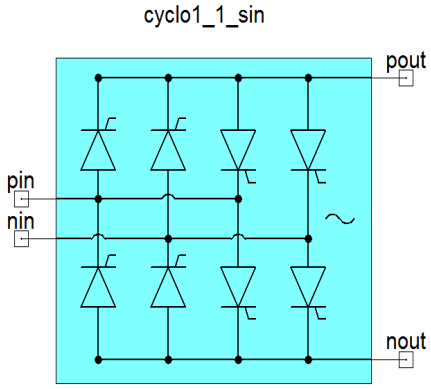

Figure 1. Component symbol

Description

The **cyclo1_1sin** represents the behavior of a single-phase to single-phase cycloconverter. The firing angle of this model is internally varied sinusoidally to reduce unwanted harmonics. The component reduces the frequency of the input voltage and will also reduce the RMS value of the output.

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Assumptions and Limitations

Top

Output frequency is less than that of the input frequency.

Alpha_o and alpha_o_o must be between 0-179.5 degrees.

Divisor must be an integer greater than zero.

Mathematical Description

Top

$$Divisor = frequency_{input} / frequency_{output}$$

Netlist Syntax

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Conservative Pins

Top

Table 1

Name	Port/Terminal description	Nature/Data type
pin	Electrical port pin	electrical
nin	Electrical port nin	electrical
pout	Electrical port pout	electrical
nout	Electrical port nout	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]

freq_in	input voltage frequency	real	60.0 [Hz]
divisor	frequency conversion divisor	real	2.0
alpha_o_o	starting initial firing angle at beginning of simulation	real	90.0 [Degrees]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
alpha_o	initial firing angle [Degrees]	Input	real

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Example

cyclo3_1half: Three-phase to single-phase half-wave cycloconverter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

cyclo3_1half

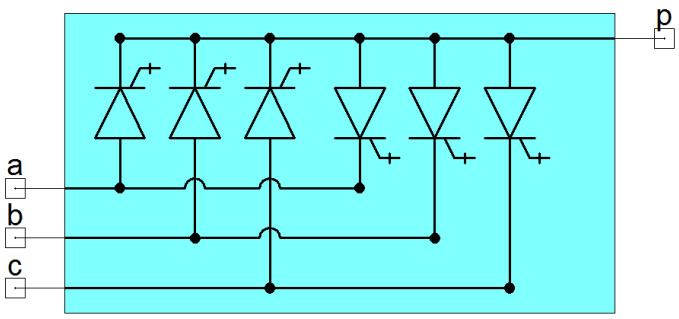

Figure 1. Component symbol

• Example

Description

The **cyclo3_1half** represents the behavior of a three-phase to single-phase cycloconverter. The component reduces the frequency of the input voltage and will also reduce the RMS value of the output.

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Assumptions and Limitations

Top

Output frequency is less than that of the input frequency.

Divisor must be an integer greater than zero.

Mathematical Description

Top

$$Divisor = frequency_{input} / frequency_{output}$$

Netlist Syntax

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Conservative Pins

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Table 1

Name	Port/Terminal description	Nature/Data type
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	electrical
p	Electrical port p	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
freq_in	input voltage frequency	real	60.0 [Hz]

divisor	frequency conversion divisor	real	2.0

Input/Output Quantities

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Example

cyclo3_3half: Three-phase to three-phase half-wave cycloconverter

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

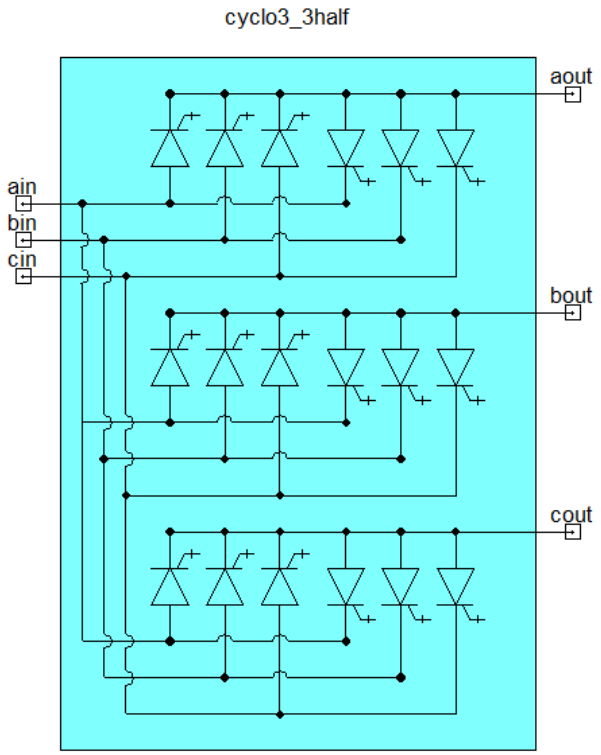

Figure 1. Component symbol

Description

The **cyclo3_3half** represents the behavior of a three-phase to three-phase half-wave cycloconverter. The component reduces the frequency of the input voltage and will also reduce the RMS value of the output.

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Assumptions and Limitations

Top

Output frequency is less than that of the input frequency.

Divisor must be an integer greater than zero.

Mathematical Description

Top

$$Divisor = frequency_{input} / frequency_{output}$$

Netlist Syntax

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Conservative Pins

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Table 1

Name	Port/Terminal description	Nature/Data type
ain	Electrical port ain	electrical
bin	Electrical port bin	electrical
cin	Electrical port cin	electrical
aout	Electrical port aout	electrical
bout	Electrical port bout	electrical
cout	Electrical port cout	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
freq_in	input voltage frequency	real	60.0 [Hz]
divisor	frequency conversion divisor	real	2.0

Input/Output Quantities

Top

Example

matrix_svpwm: Three-phase matrix converter with direct space vector control

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

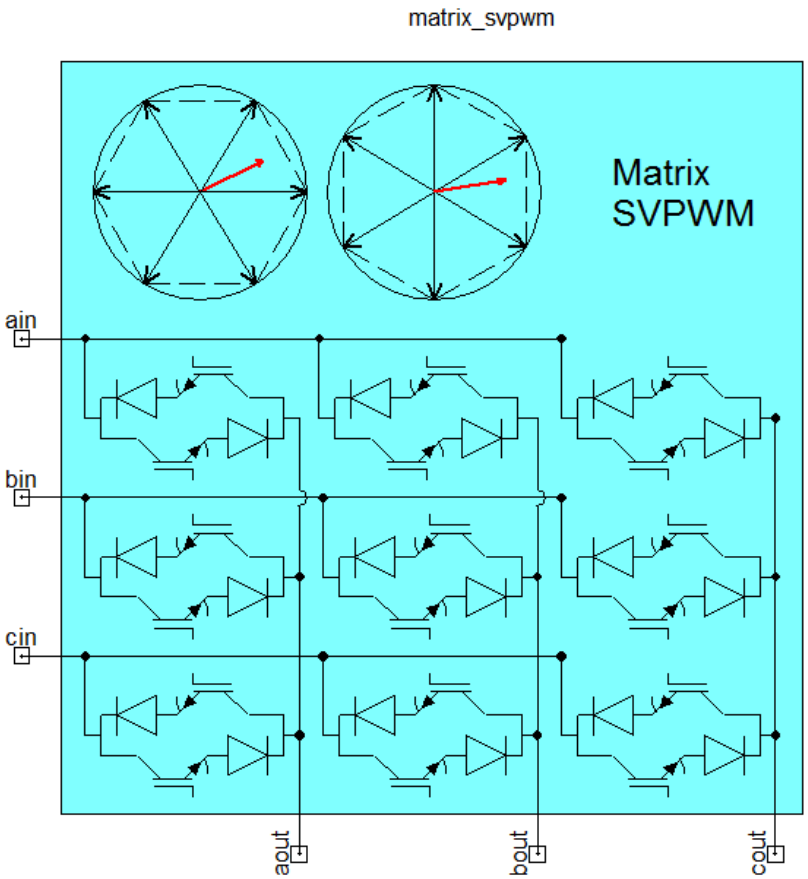

Figure 1. Component symbol

Description

The **matrix_svpwm** represents the behavior of a three-phase matrix converter. The control signals are generated through the direct space vector method as described in the references and are internally generated.

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Assumptions and Limitations

Output voltage amplitude cannot exceed input amplitude.

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Mathematical Description

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Table 1

Name	Port/Terminal description	Nature/Data type
ain	Electrical port ain	electrical
bin	Electrical port bin	electrical
cin	Electrical port cin	electrical

aout	Electrical port aout	electrical
bout	Electrical port bout	electrical
cout	Electrical port cout	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3[Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
v_in_ phase	phase reference of the input voltage	real	0.0 [Degrees]
v_out_ phase	phase reference of the output voltage	real	0.0 [Degrees]
phi_i	phase difference of input voltage and current	real	0.0 [Radians]
sw_freq	switching frequency	real	0.0 [Hz]
dead_time	dead time of the switching elements	real	0.0 [s]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
v_in_amplitude	input voltage amplitude [V]	Input	real
v_in_freq	input voltage frequency [Hz]	Input	real
v_out_amp	output voltage amplitude [V]	input	real
v_out_freq	output voltage frequency [Hz]	input	real

Top

Example

[1] J. Vadillo, J.M. Echeverria, L. Fontan, M. Martinez-Iturralde and I. Elosegui, “Modeling and Simulation of a Direct Space Vector Modulated Matrix Converter using different Switching Strategies,” IEEE Xplore, 29-Jul-2011. [Online]. Available: http://iee-explore.ieee.org/stamp/stamp.jsp?arnumber=5986703. [Accessed: 14-Jul-2008].

[2] J. Rodriguez, M. Rivera, J. W. Kholar, and P. W. Wheeler, “A Review of Control and Modulation Methods for Matrix Converter,” IEEE Xplore, 04-Oct-2011. [Online]. Available: http://iee-explore.ieee.org/stamp/stamp.jsp?arnumber=5986703. [Accessed: 14-Jul-2017].

[3] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and Alejandro Weinstein, “Matrix Converters: A Technology Review,” IEEE Xplore, 2002. [Online]. Available: http://iee-explore.ieee.org/document/993260/. [Accessed: 14-Jul-2008].

matrix_venturini: Three-phase matrix converter with venturini control

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

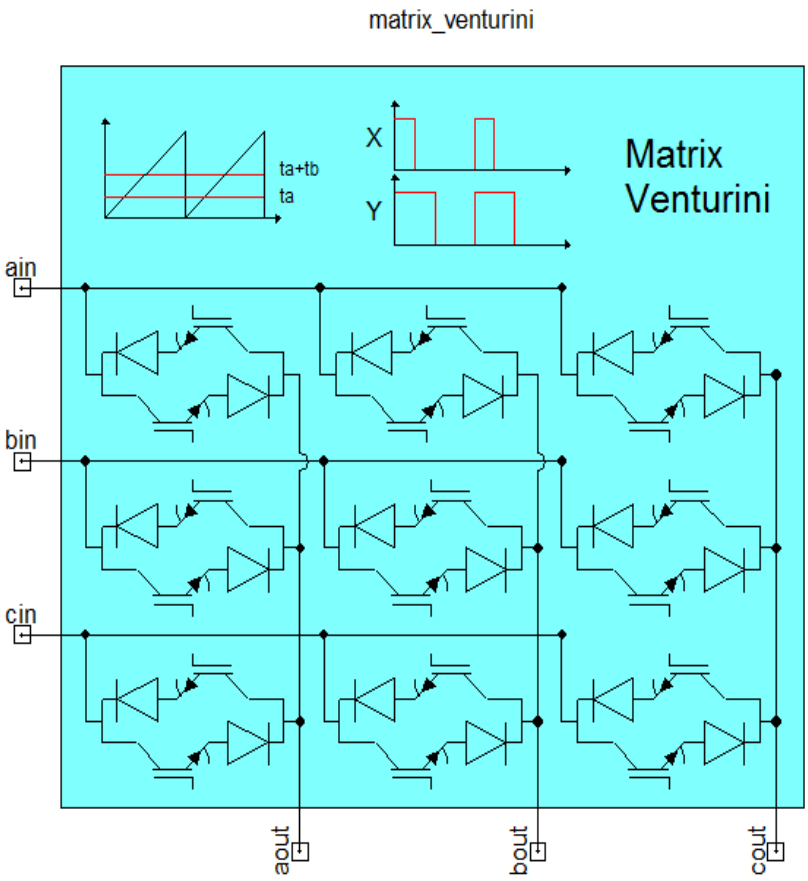

Figure 1. Component symbol

Description

The **matrix_venturini** represents the behavior of a three-phase matrix converter. The control signals are generated through the venturini method as described in the references and are internally generated.

Top

Assumptions and Limitations

When using nothird architecture, trans_ratio cannot exceed 0.5.

When using thirdharm architecture, trans_ratio cannot exceed 0.86.

Top

Mathematical Description

$$trans\_ratio = Output\ Voltage\ Amplitude / Input\ Voltage\ Amplitude$$

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Netlist Syntax

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Table 1

Name	Port/Terminal description	Nature/Data type
ain	Electrical port ain	electrical
bin	Electrical port bin	electrical
cin	Electrical port cin	electrical
aout	Electrical port aout	electrical
bout	Electrical port bout	electrical
cout	Electrical port cout	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk res-istance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse res-	resistance	100.0e3 [Ohm]

	istance		
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3[Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
phase_ shift	phase reference of the output voltage	real	0.0 [Degrees]
freq_sw	switching frequency	real	0.0 [Hz]

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
trans_ratio	transfer ratio	Input	real
freq_in	input voltage frequency [Hz]	Input	real
freq_out	output voltage frequency [Hz]	input	real
v_in_amp	input voltage amplitude [V]	input	real

Top

Example

[1] J. Rodriguez, M. Rivera, J. W. Kholar, and P. W. Wheeler, “A Review of Control and Modulation Methods for Matrix Converter,” IEEE Xplore, 04-Oct-2011. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5986703. [Accessed: 14-Jul-2017].

[2] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and Alejandro Weinstein, “Matrix Converters: A Technology Review,” IEEE Xplore, 2002. [Online]. Available: http://ieeexplore.ieee.org/document/993260/. [Accessed: 14-Jul-2008].

[3] H. Karaca, and R. Akkaya, “Control of Venturini Method Based Matrix Converter in Input Voltage Variations,” IENG, 2009. [Online]. Available: http://www.iaeng.org/publication/IMECS2009/IMECS2009_pp1412-1416.pdf. [Accessed: 14-Jul-2008].

ttype: Three-phase three-level T-Type inverter

Library: Power System	Modeling Language:	Version Number: Twin

VHDLAMS	VHDL-AMS	Builder 2024.2

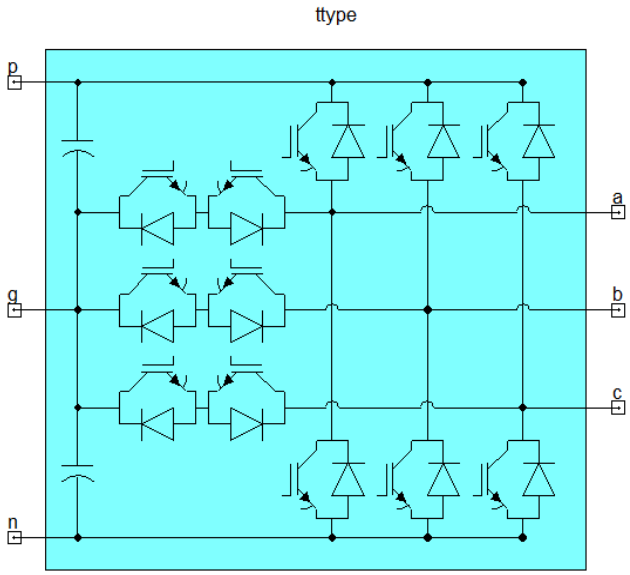

Figure 1. Component symbol

Description

The **ttype** represents the behavior of a three-phase, three-level, T-Type inverter.

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Assumptions and Limitations

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
g	Electrical port g	electrical
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk resistance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse resistance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3 [Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_v0	capacitance initial voltage	voltage	0.0 [V]
c_use_v0	use initial capacitance	Boolean	false

	voltage or not		

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
c_val	capacitance value [F]	Input	capacitance
ctrl1	control input signal 1	Input	real
ctrl2	control input signal 2	input	real
ctrl3	control input signal 3	input	real
ctrl4	control input signal 4	input	real
ctrl5	control input signal 5	input	real
ctrl6	control input signal 6	input	real
ctrl7	control input signal 7	input	real
ctrl8	control input signal 8	input	real
ctrl9	control input signal 9	input	real
ctrl10	control input signal 10	input	real
ctrl11	control input signal 11	input	real
ctrl12	control input signal 12	input	real

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Example

vienna: Fully-controlled three-phase vienna rectifier

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

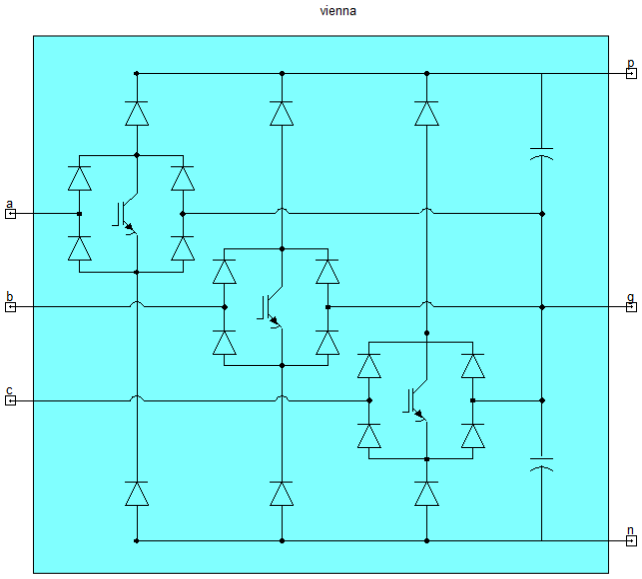

Figure 1. Component symbol

Description

The **vienna** represents the behavior of a three-phase vienna inverter. Gating signals for the switching elements are generated internally.

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Assumptions and Limitations

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Mathematical Description

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
n	Electrical port n	electrical
g	Electrical port g	electrical
a	Electrical port a	electrical
b	Electrical port b	electrical
c	Electrical port c	electrical

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
sw_vf	igbt/mosfet forward voltage	voltage	0.8 [V]
sw_rb	igbt/mosfet bulk res-istance	resistance	1.0e-3 [Ohm]
sw_rr	igbt/mosfet reverse res-istance	resistance	100.0e3 [Ohm]
sw_isat	igbt/mosfet saturation current	current	1.0e-12 [A]
sw_vt	igbt/mosfet thermal voltage	voltage	35.0e-3 [V]
diode_vf	diode forward voltage	voltage	0.8 [V]
diode_rb	diode bulk resistance	resistance	1.0e-3[Ohm]
diode_rr	diode reverse resistance	resistance	100.0e3 [Ohm]
diode_isat	diode saturation current	current	1.0e-12 [A]
diode_vt	diode thermal voltage	voltage	35.0e-3 [V]
c_v0	capacitance initial	voltage	0.0 [V]

	voltage		
c_use_v0	use initial capacitance voltage or not	Boolean	false
c_val	capacitance value [F]	Input	capacitance

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
modu_ind_ref	modulation index reference	Input	real
freq_in	Phase of PWM reference signal [Hz], should be the same as frequency of AC source voltage	Input	real
phase_ref	Phase of PWM reference signal [degree], should be the same as phase of AC source voltage	Input	real
sw_freq	Frequency of PWM carrier [Hz]	Input	real
dead_time	Switching deadtime [s]	Input	real

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Example

[1] J. W. Kolar and F. C. Zach, “A Novel Three-Phase Utility Interface Minimizing Line Current Harmonics of High-Power Telecommunications Rectifier Modules,” IEEE Xplore, 06-Aug-2002. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=396642. [Accessed: 29-Jun-2017].

[2] J. W. Kolar, H. Sree, U. Drofenik, N. Mohan, and F. C. Zach, “A Novel Three-Phase Three-Switch Three-Level High Power Factor SEPIC-Type AC-to-DC Converter,” IEEE Xplore. [Online]. Available: http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=575655. [Accessed: 29-Jun-2017].

[3] H. Vahedi, P.-A. Labbè, and K. Al-Haddad, “Single-Phase Single-Switch Vienna Rectifier as Electric Vehicle PFC Battery Charger,” IEEE Xplore, 17-Dec-2015. [Online]. Available: http://ieeexplore.ieee.org/document/7353019/. [Accessed: 29-Jun-2017].

EMI EMC

The EMI EMC sub-library consists of Frequency Dependent Elements, impedance stabilization networks and line impedance stabilization networks components for power systems, and it contains:

- Frequency dependent elements
- Impedance stabilization networks
- Line impedance stabilization networks
- Three phase line impedance stabilization network

Frequency Dependent Elements

The Frequency Dependent Elements consists of frequency dependent RLC with typical topology for power systems and it contains:

- Frequency dependent resistance
- Frequency dependent inductance
- Frequency dependent capacitance

c_freq: Frequency dependent capacitance

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

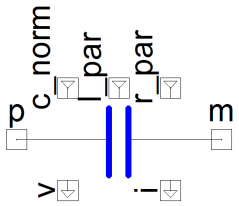

Figure 1. Component symbol

• Description

• Assumptions and Limitations

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Description

The **c_freq** represents the behavior of a simplified version of the non-ideal capacitor with a series connected lead inductance and resistance.

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
m	Electrical port m	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
v_norm0	initial voltage on the nominal capacitance	voltage	0.0 [V]
i_par0	initial current on the parasitic inductance	current	0.0 [A]
use_initial	use the initial values or not	Boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
L_par	parasitic series inductance value, default value is 6.0e-8 [H]	Input	inductance
R_par	parasitic series resistance value, default value is 1.0e-2 [Ohm]	Input	resistance
C_norm	nominal capacitance value, default value is 1.0e-6 [F]	Input	capacitance
V	voltage measurement	output	voltage
I	current measurement	output	current

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Example

Frequency Dependent Elements Example

l_freq: Frequency dependent inductance

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

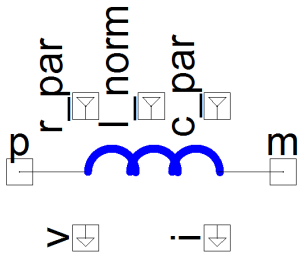

Figure 1. Component symbol

- Description
- Assumptions and Limitations
- Mathematical Description
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- Conservative Pins
- Parameters

Description

The **l_freq** represents a simplified version of the non-ideal inductor with a series connected parasitic resistance and a parallel connected parasitic capacitance between turns of wire in the windings.

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
m	Electrical port m	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
v_par0	initial voltage on the parasitic capacitance	voltage	0.0 [V]
i_norm0	initial current on the norminal inductance	current	0.0 [A]
use_initial	use the initial values or not	Boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
L_norm	nominal inductance value, default value is 1.2e-6 [H]	Input	inductance
R_par	parasitic series resistance value, default value is 1.0e-3 [Ohm]	Input	resistance
C_par	parasitic capacitance value, default value is 1.0e-9 [F]	Input	capacitance
V	voltage measurement	output	voltage
I	current measurement	output	current

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Example

Frequency Dependent Elements Example Example

r_freq: Frequency dependent resistance

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

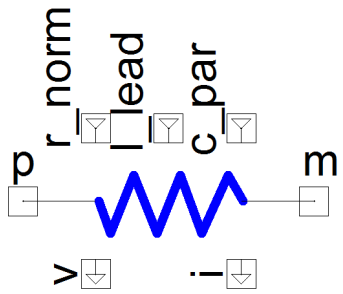

Figure 1. Component symbol

- Description
- Assumptions and Limitations
- Mathematical Description
- Netlist Syntax
- Conservative Pins

Description

The **r_freq** represents the simplified version of the frequency dependent resistor with equivalent series inductance (ESL) and parasitic shunt capacitance. The parasitic shunt capacitance is a parallel combination of the lead capacitance and the stray leakage capacitance.

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Table 1

Name	Port/Terminal description	Nature/Data type
p	Electrical port p	electrical
m	Electrical port m	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
v_par0	initial voltage on the parasitic capacitance	voltage	0.0 [V]
i_par0	initial current on the parasitic inductance	current	0.0 [A]
use_initial	use the initial values or	Boolean	true

	not		

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
L_lead	equivalent series induct-ance value, default value is 1.0e-6 [H]	Input	inductance
R_norm	nominal resistance value, default value is 1.0e3 [Ohm]	Input	resistance
C_par	parasitic capacitance value, default value is 1.0e-9 [F]	Input	capacitance
V	voltage measurement	output	voltage
I	current measurement	output	current

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Example

Frequency Dependent Elements Example

lisn_3phase: Three Phase Line Impedance Stabilization Networks

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

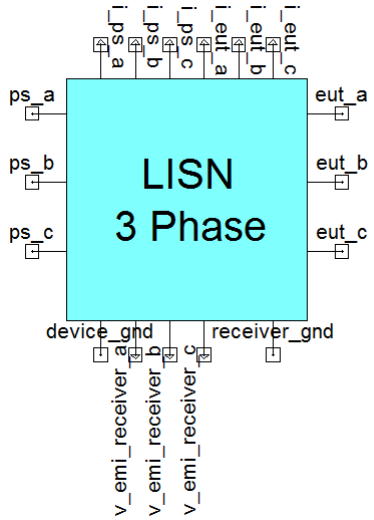
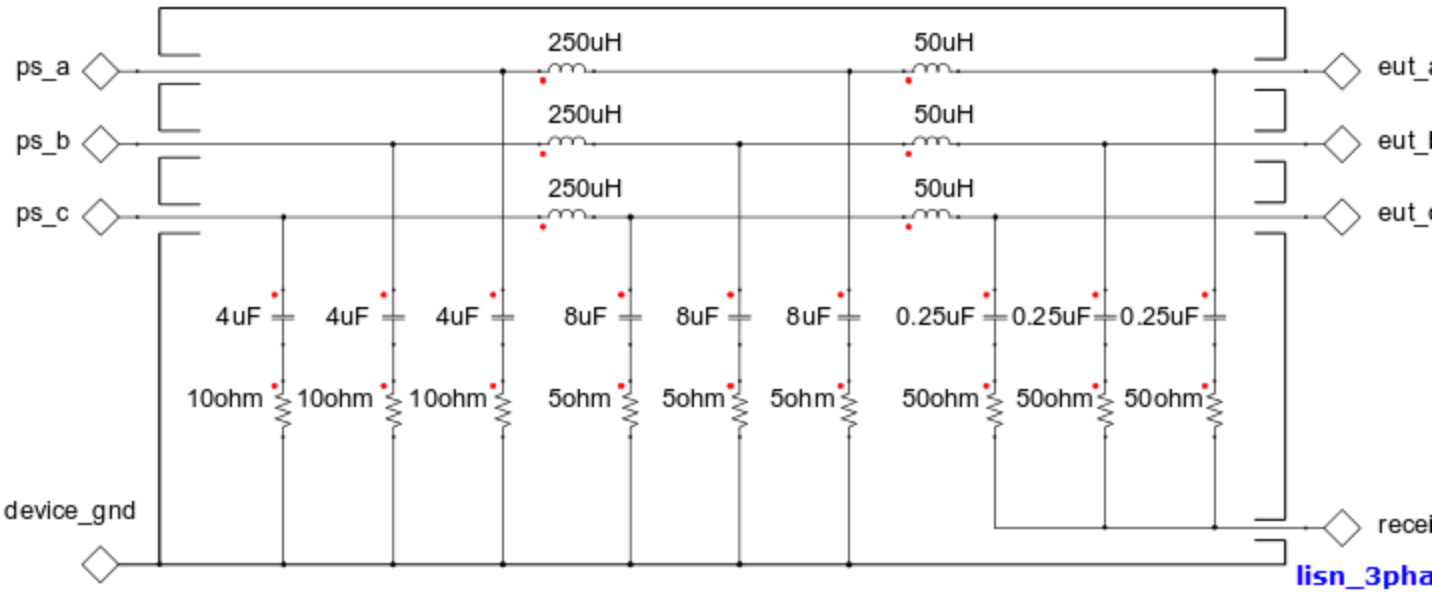


Figure 1. Component symbol

Description

The **lisn_3phase** represents the 3 phase LISN following the reference paper, Figure 1, with 50 Ohm loads included on the measurement. The EMI receiver voltage is provided instead of a measurement port. The equivalent circuit for this model is shown below.



@reference

M. L. Heldwein, J. Biela, H. Ertl, T. Nussbaumer and J.W. Kolar, "Novel Three-Phase CM/DM Conducted Emission Separator", IEEE Transactions on Industrial Electronics, ol. 56, No. 9, P3693-3703.

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Conservative Pins

Name	Port/Terminal description	Nature/Data type
PS_A	Electrical port connects to power source phase A	electrical
PS_B	Electrical port connects to power source phase B	electrical
PS_C	Electrical port connects to power source phase C	electrical
EUT_A	Electrical port connects to equipment under test phase A	electrical
EUT_B	Electrical port connects to equipment under test phase B	electrical
EUT_C	Electrical port connects to equipment under test phase C	electrical
Receiver_GND	Electrical port connects to receiver ground	electrical
Device_GND	Electrical port connects to device ground	electrical

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Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
I_PS_A	Current measurement of power source side phase A	Out	current
I_PS_B	Current meas-	Out	current

	urement of power source side phase B		
I_PS_C	Current measurement of power source side phase C	Out	current
I_EUT_A	Current measurement of equipment under test side phase A	Out	current
I_EUT_B	Current measurement of equipment under test side phase B	Out	current
I_EUT_C	Current measurement of equipment under test side phase C	Out	current
V_EMI_Receiver_A	Voltage measurement of EMI receiver phase A	Out	voltage
V_EMI_Receiver_B	Voltage measurement of EMI receiver phase B	Out	voltage
V_EMI_Receiver_C	Voltage measurement of EMI receiver phase C	Out	voltage

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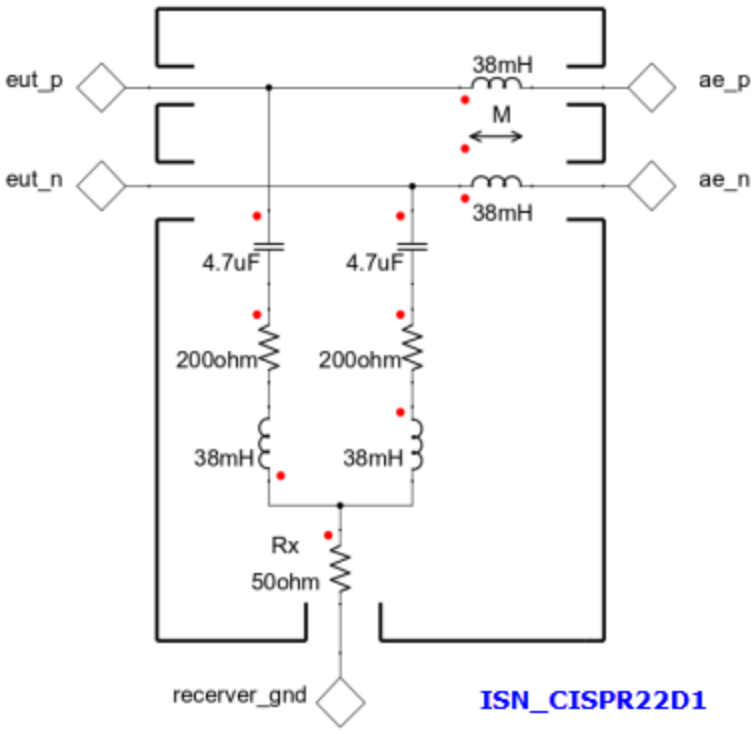
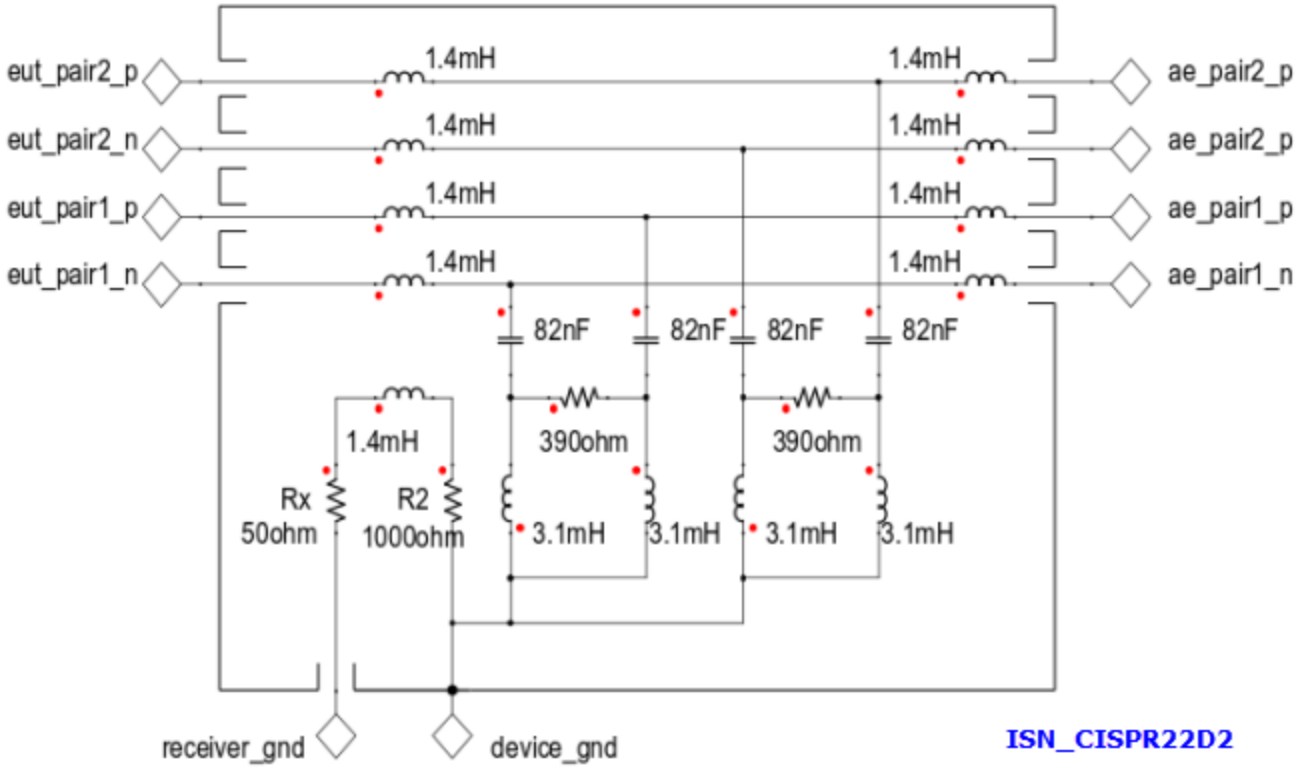
Impedance Stabilization Networks

The **ISN** sub-library represents the impedance stabilization networks defined by standard CISPR22 Annex D1-D7 (version 2006), all the parameters and settings are followed the values given by the standard. It contains the components listed below.

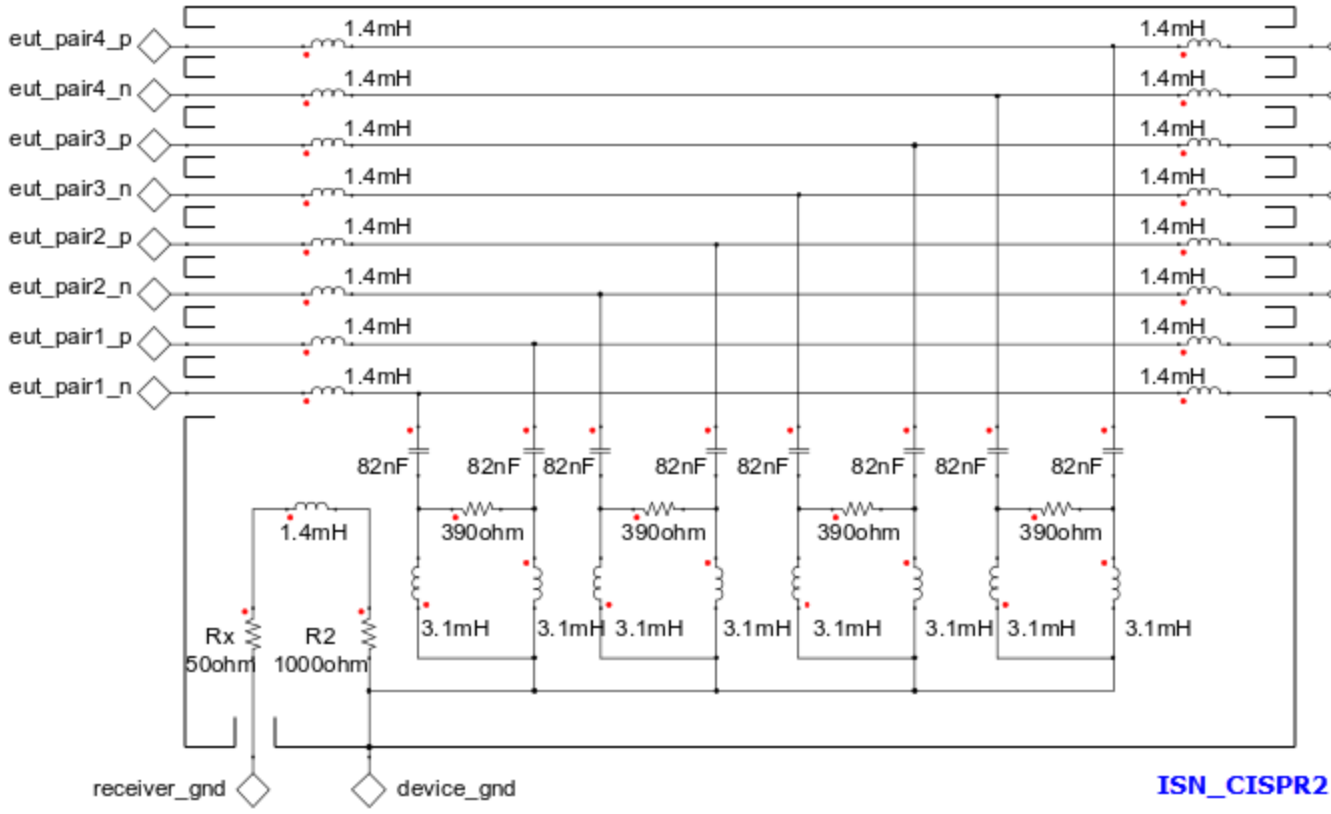
ISN_CISPR22D1: This model represents the ISN for use with unscreened single balanced pairs, defined by standard CISPR22 Annex D1 (version 2006). A Zcat connects to the EUT_N may needed to represents the unbalance network and the LCL may need to be adjusted to the value specified to the Standard. The equivalent circuit for this model is shown below.



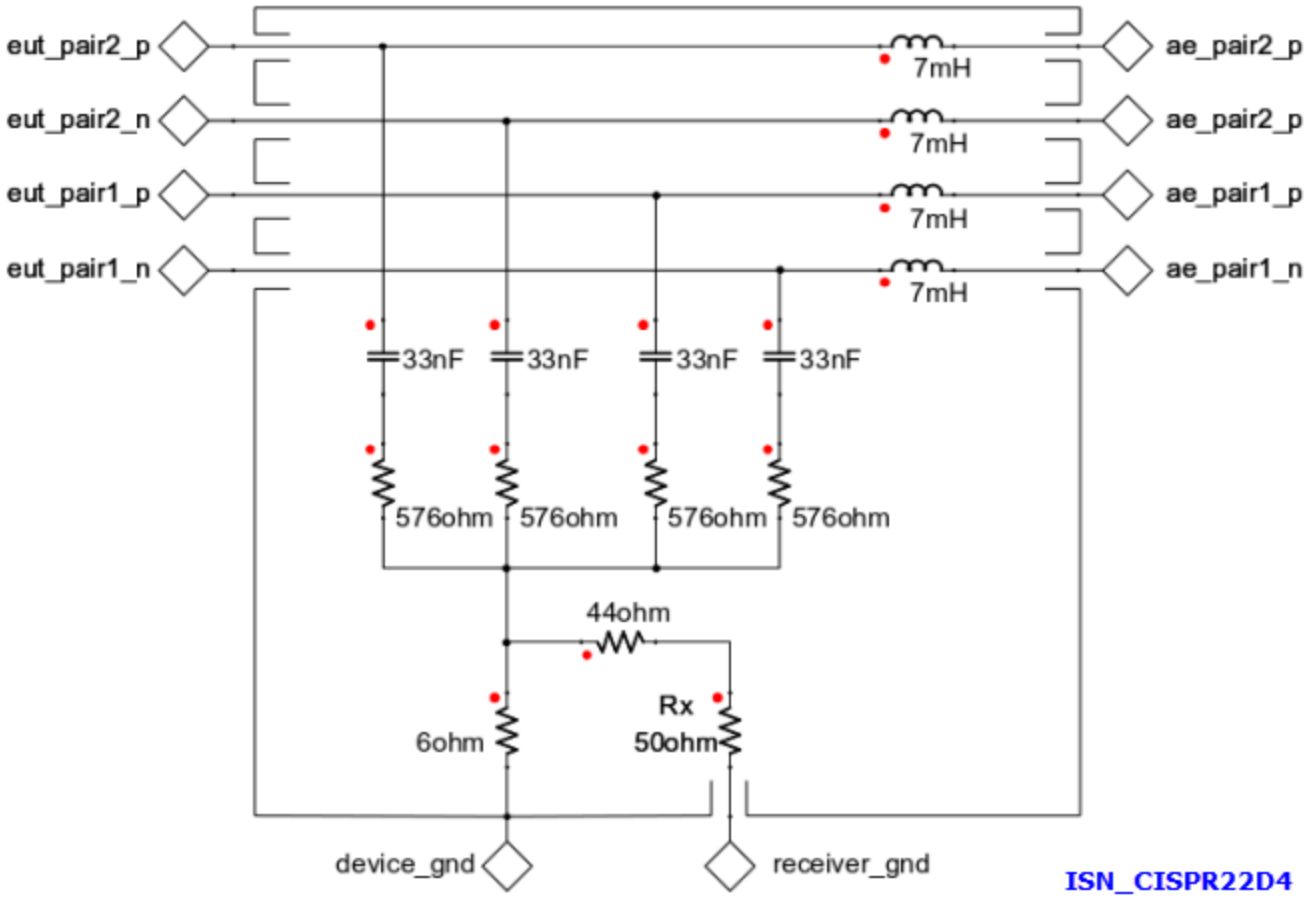
ISN_CISPR22D2: This model represents the ISN with high longitudinal conversion loss (LCL)for use with either one or two unscreened balanced pairs, defined by standard CISPR 22 Annex D2 (version 2006). Zcats connect to the EUT_Pair1_N and/or EUT_ Pair2_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. The equivalent circuit for this model is shown below.



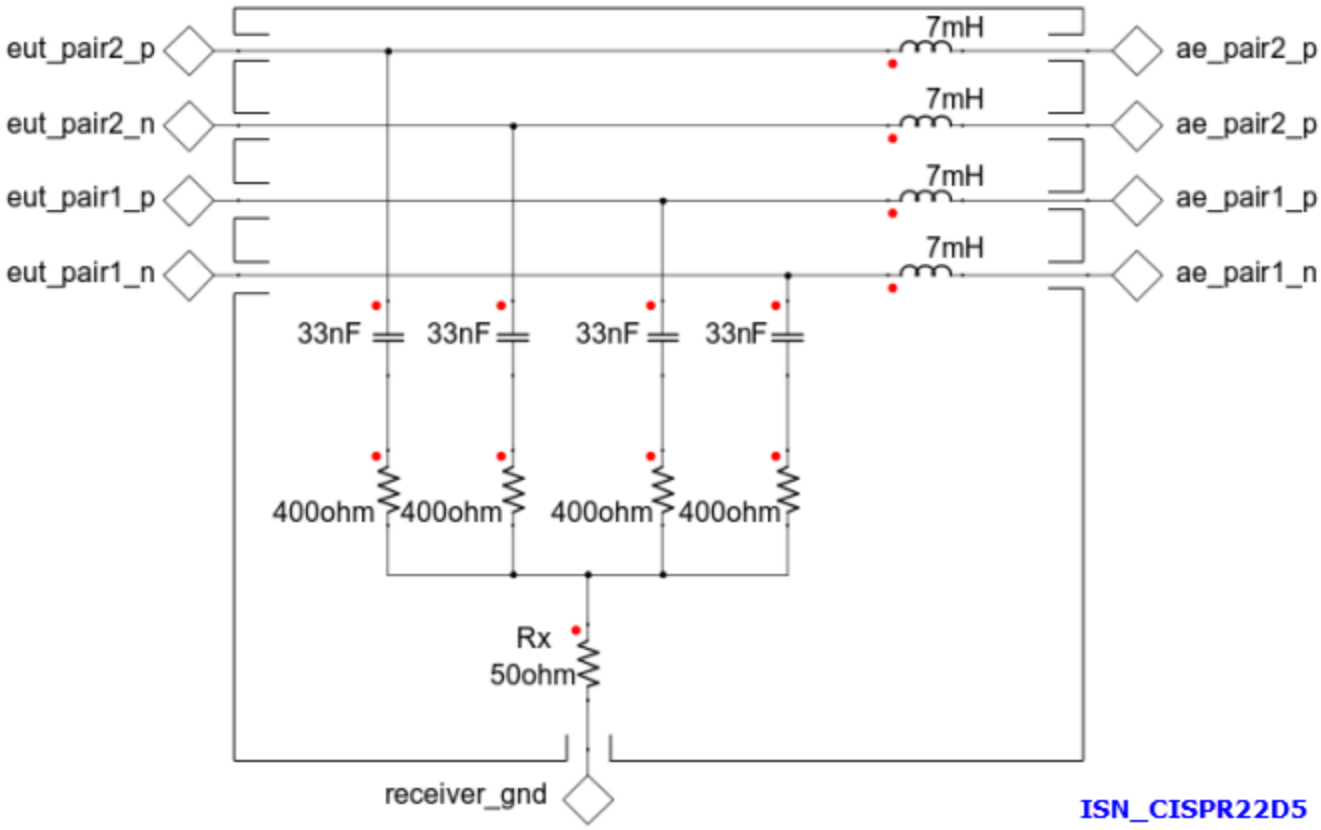
ISN_CISPR22D3: This model represents the ISN with high longitudinal conversion loss (LCL)for use with either one, two, three, or four unscreened balanced pairs, defined by standard CISPR 22 Annex D3 (version 2006). Zcats connect to the EUT_Pair1_N, EUT_ Pair2_N, EUT_Pair3_N and/or EUT_Pair4_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. The equivalent circuit for this model is shown below.



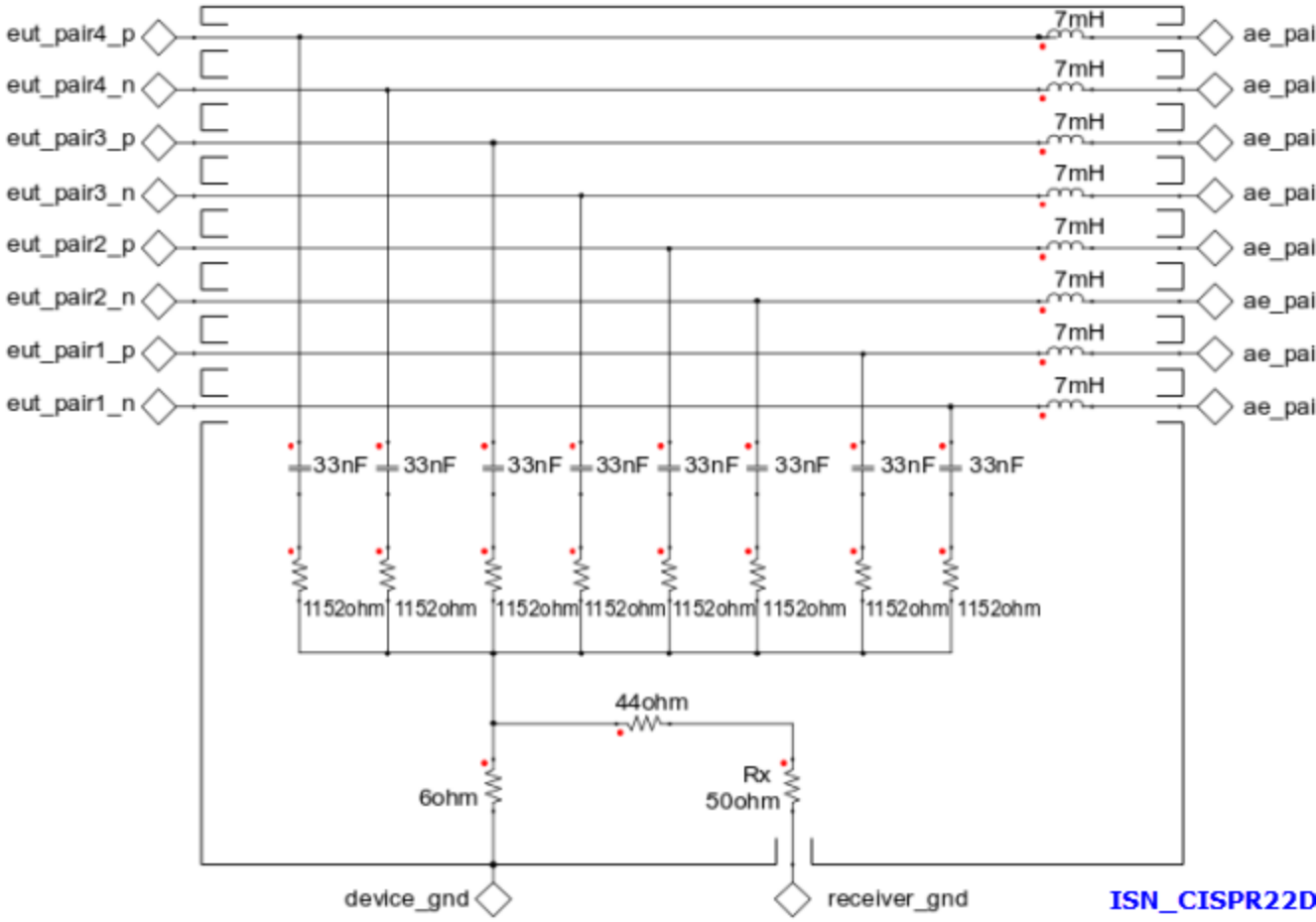
ISN_CISPR22D4: This model represents the ISN, including a 50 Ohm source matching network at the voltage measuring port, for use with two unscreened balanced pairs, defined by standard CISPR 22 Annex D4 (version 2006). Zcats connect to the EUT_ Pair1_N and/or EUT_Pair2_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. This ISN must not be used to measure common mode disturbances on unscreened pair cables connected to telecommunication ports that employ only one active unscreened balanced pair. The equivalent circuit for this model is shown below.



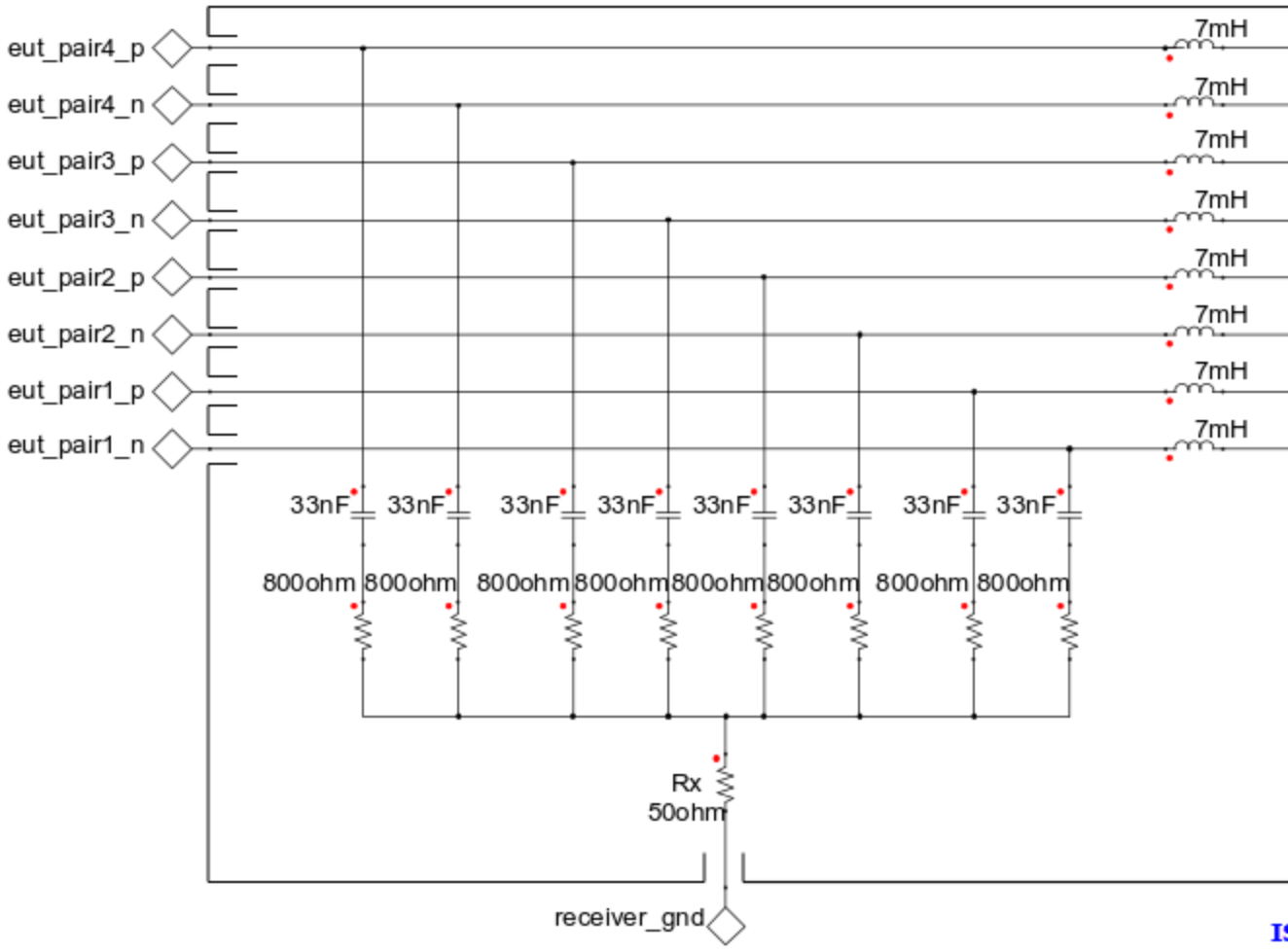
ISN_CISPR22D5: This model represents the ISN for use with two unscreened balanced pairs, defined by standard CISPR 22 Annex D5 (version 2006). Zcats connect to the EUT_Pair1_N and/or EUT_Pair2_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. This ISN must not be used to measure common mode disturbances on unscreened pair cables connected to telecommunication ports that employ only one active unscreened balanced pair. The equivalent circuit for this model is shown below.



ISN_CISPR22D6: This model represents the ISN, including a 50 Ohm source matching network at the voltage measuring port, for use with four unscreened balanced pairs, defined by standard CISPR 22 Annex D6 (version 2006). Zcats connect to the EUT_ Pair1_N, EUT_Pair2_N, EUT_Pair3_N and/or EUT_Pair4_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. This ISN must not be used to measure common mode disturbances on unscreened pair cables connected to telecommunication ports that employ only one active unscreened balanced pair. The equivalent circuit for this model is shown below.



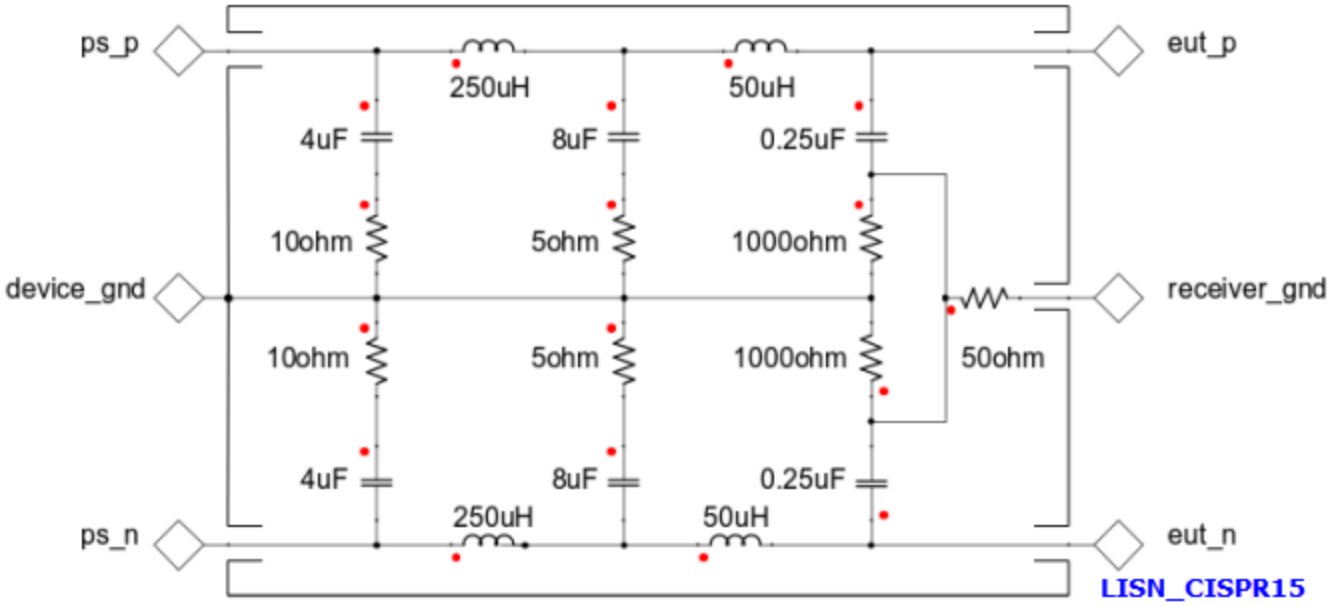
ISN_CISPR22D7: This model represents the ISN for use with four unscreened balanced pairs, defined by standard CISPR 22 Annex D7 (version 2006). Zcats connect to the EUT_Pair1_N, EUT_Pair2_N, EUT_Pair3_N and/or EUT_Pair4_N may be needed to represents the unbalance network and the LCL may need to be adjusted to the values specified to the Standard. This ISN must not be used to measure common mode disturbances on unscreened pair cables connected to telecommunication ports that employ only one active unscreened balanced pair. The equivalent circuit for this model is shown below.



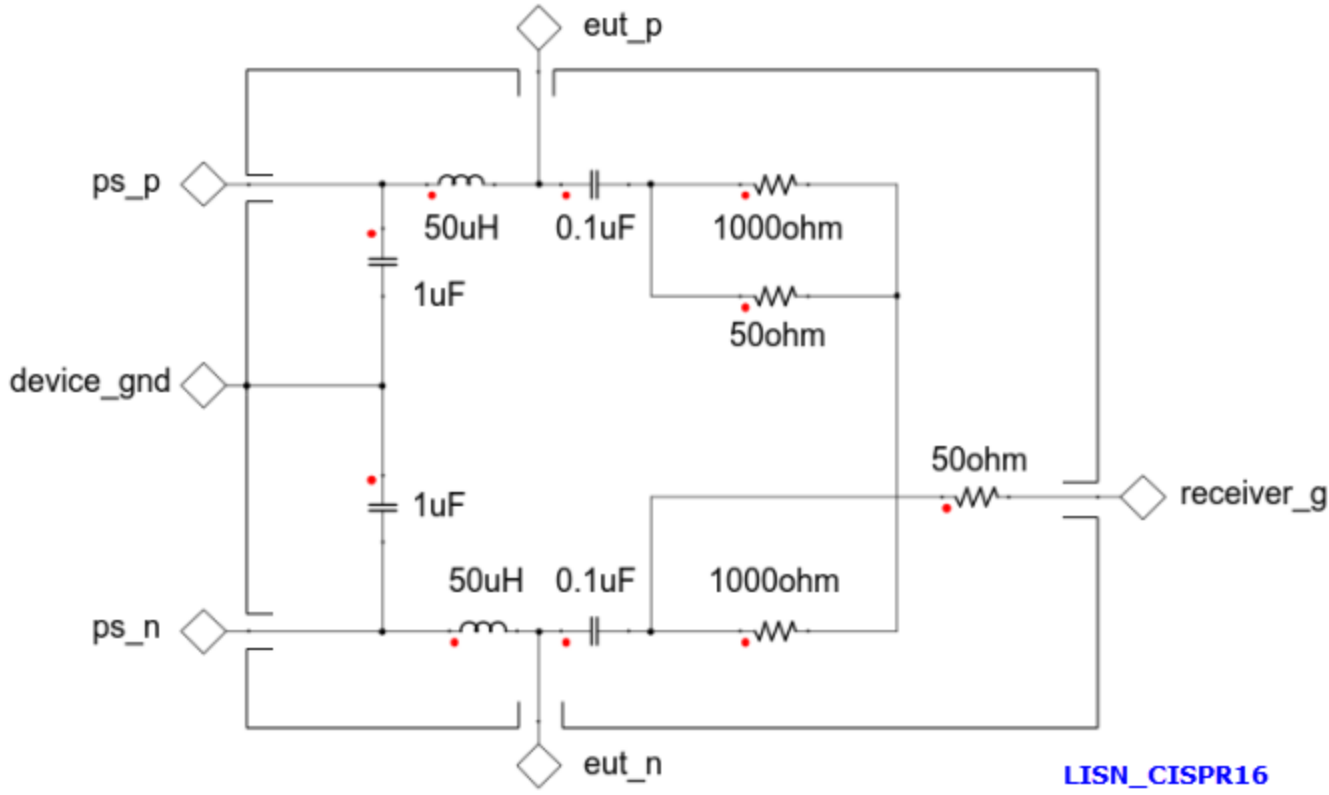
Line Impedance Stabilization Networks

The **LISN** sub-library represents the line impedance stabilization networks defined by different standards, all the parameters and settings are followed the values given by the standards. It contains the components listed below.

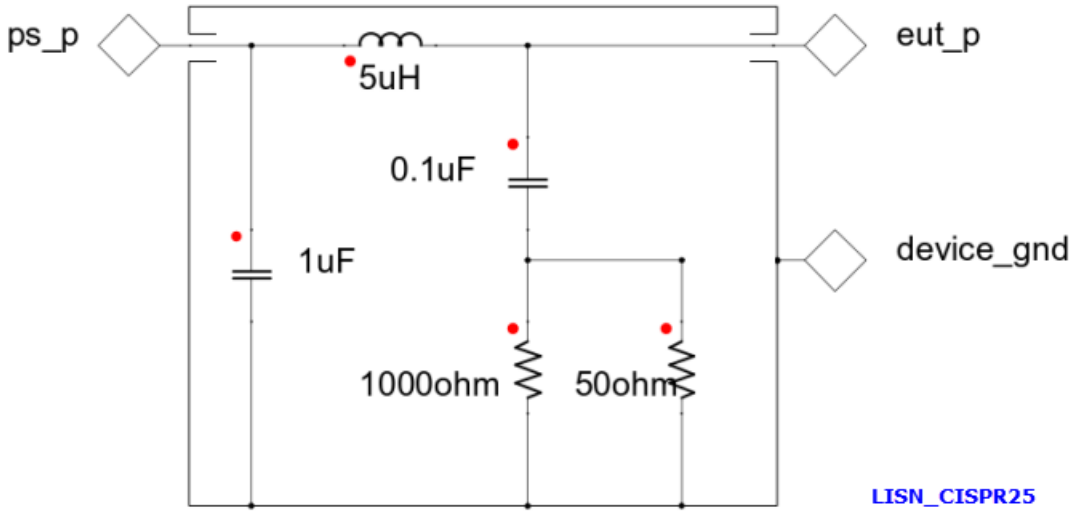
LISN_CISPR15: This model represents the 50 Ohm, 50 uH + 5 Ohm LISN circuit originated with VDE conducted emissions testing. It is also the LISN required for CISPR 15 testing of Luminaries. Compare to CISPR 16, it includes additional inductors and capacitors for filtering and has an operating frequency of 9 kHz - 30 MHz. The equivalent circuit for this model is shown below.



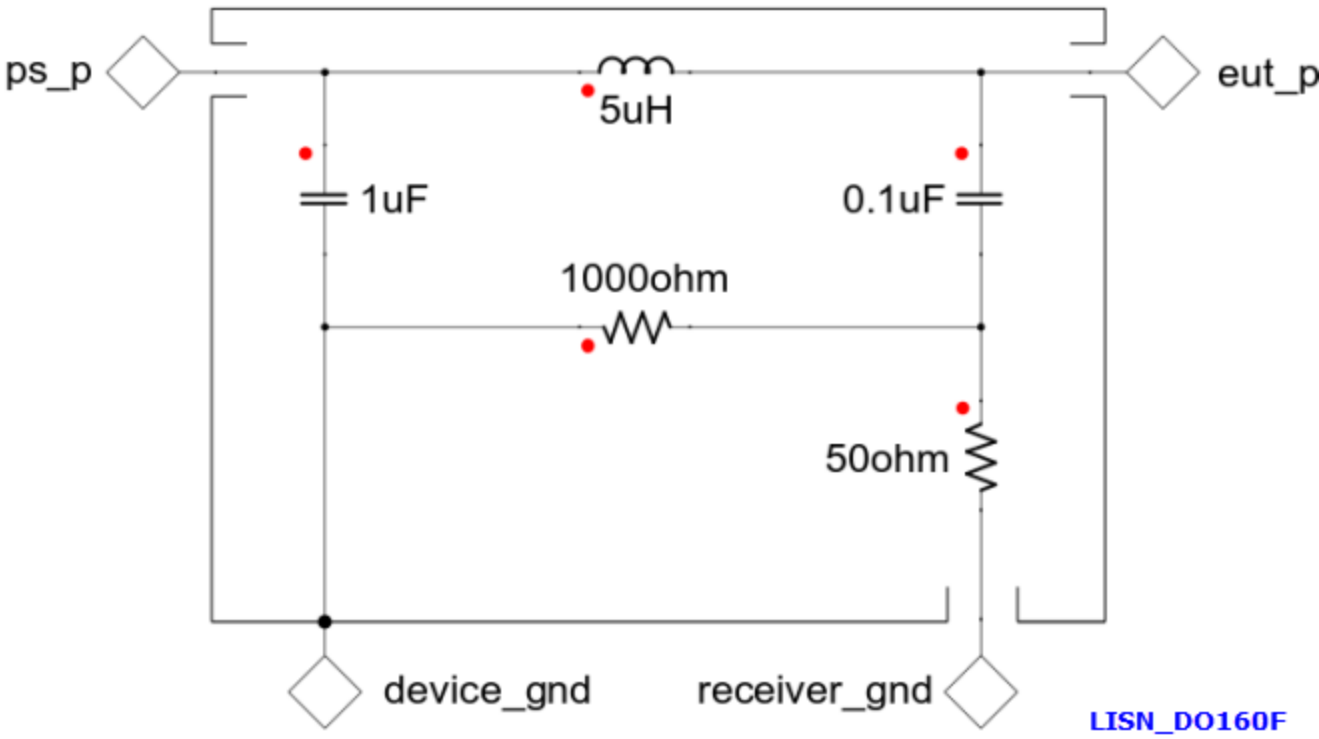
LISN_CISPR16: This model represents the 50 Ohm, 50 uH LISN circuit defined in CISPR 16-1-2. 2006. The equivalent circuit for this model is shown below.



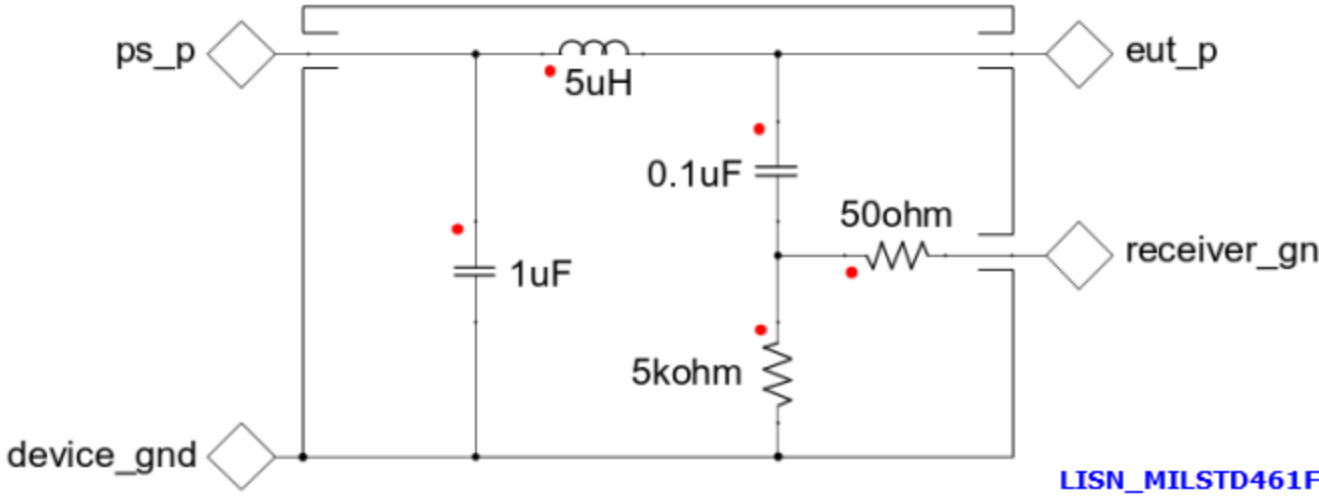
LISN_CISPR25: This model represents the LISN for use with frequency range from 0.1 MHz to 100 MHz, defined by standard CISPR-25 E.2, version 2008, with a 50 Ohm load included on the measurement. The EMI receiver voltage is provided instead of a measurement port. The equivalent circuit for this model is shown below.



LISN_DO160F: This model represents the LISN for use with frequency range from 10 KHz to 400 MHz, defined by standard RTCA DO-160F. The equivalent circuit for this model is shown below.



LISN_MILSTD461F: This model represents the LISN for use with frequency range from 10 KHz to 10 MHz, defined by standard MIL-STD 461F Annex A-2. The equivalent circuit for this model is shown below.



Transformer

The Transformer sublibrary consists of non-ideal linear transformer and topology for power systems, and it contains:

- Linear non-ideal primary winding
- Linear non-ideal secondary winding
- Linear non-ideal transformer with Delta-Delta connection
- Linear non-ideal transformer with Wye-Wye connection
- Linear non-ideal transformer with Wye-Delta connection, lag 30 degree
- Linear non-ideal transformer with Wye-Delta connection, lead 30 degree
- Linear non-ideal transformer with Delta-Wye connection, lag 30 degree
- Linear non-ideal transformer with Delta-Wye connection, lead 30 degree
- Linear non-ideal transformer with Delta-Delta-Wye connection, lag 30 degree
- Linear non-ideal transformer with Delta-Delta-Wye connection, lead 30 degree
- Linear non-ideal transformer with Wye-Delta-Wye connection, lag 30 degree
- Linear non-ideal transformer with Wye-Delta-Wye connection, lead 30 degree

pwinding: Linear non-ideal primary winding

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

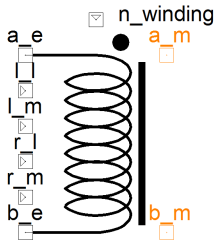


Figure 1. Component symbol

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- Conservative Pins
- Parameters
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Description

The **pwinding** represents the behavior of a linear non-ideal primary winding with consideration of winding leakage and core magnetization based on proper parameterized equivalent electrical components on the electrical winding.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_e	Electrical port a_e	electrical
b_e	Electrical port b_e	electrical
a_m	Magnetic port a_m	magnetic
b_m	Magnetic port b_m	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux.	real	0.0 [Wb]
il_0	initial current for leakage inductance	current	0.0 [A]
im_0	initial current for mag-netization inductance	current	0.0 [A]

use_i0	use the initial values or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_l	Leakage resistance [Ohm]	input	resistance
l_l	Leakage inductance [H]	input	inductance
r_m	magnetization resistance [Ohm]	input	resistance
l_m	magnetization inductance [H]	input	inductance
n_wind-ing	Number of winding turns.	Input	Real

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Example

Simple Transformer Example

swinding: Linear non-ideal secondary winding

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

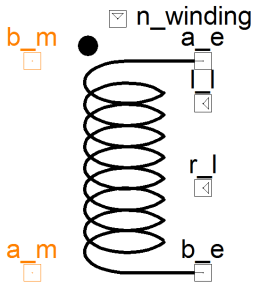

Figure 1. Component symbol

- Description
- Assumptions and Limitations
- Mathematical Description
- Netlist Syntax
- Conservative Pins

Description

The **swinding** represents the behavior of a linear non-ideal secondary winding with consideration of winding leakage.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_e	Electrical port a_e	electrical
b_e	Electrical port b_e	electrical
a_m	Magnetic port a_m	magnetic
b_m	Magnetic port b_m	magnetic

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux.	real	0.0 [Wb]
il_0	initial current for leakage inductance	current	0.0 [A]

use_i0	use the initial values or not	Boolean	false

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_l	Leakage resistance [Ohm]	input	resistance
l_l	Leakage inductance [H]	input	inductance
n_wind-ing	Number of winding turns.	Input	Real

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Example

Simple Transformer Example

transformer_dd: Linear non-ideal transformer with Delta-Delta connection

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

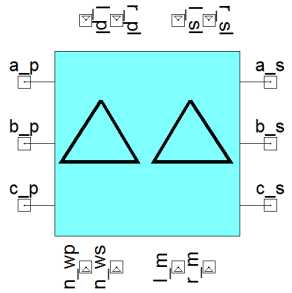

Figure 1. Component symbol

Description

The **transformer_dd** represents the behavior of a linear non-ideal three phase transformer with Delta-Delta connection, includes linear winding leakage and linear core magnetization effects.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]

ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage inductance.	Input	inductance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Delta Delta Connection Example

transformer_ddy_lag30: Linear non-ideal transformer with Delta-Delta-Wye connection, lag 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

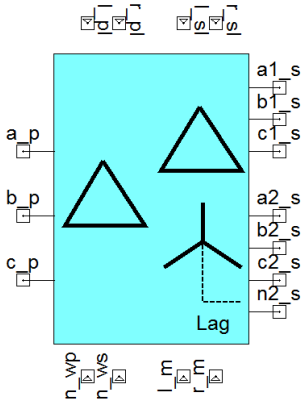

Figure 1. Component symbol

Description

The **transformer_ddy_lag30** represents the behavior of a linear non-ideal three phase transformer with Delta as the primary windings connection, two secondary connections with Delta and Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary wye voltage lag the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
a1_s	Electrical port a1_s, secondary side Delta connection phase A	electrical
b1_s	Electrical port b1_s, secondary side Delta connection phase B	electrical
c1_s	Electrical port c1_s, secondary side Delta connection phase C	electrical
a2_s	Electrical port a2_s, secondary side Wye connection phase A	electrical
b2_s	Electrical port b2_s, secondary side Wye connection phase B	electrical
c2_s	Electrical port c2_s, secondary side Wye connection phase C	electrical
n2_s	Electrical port n2_s, secondary side Wye connection neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on sec-	current	0.0 [A]

	ondary windings		
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Delta-Delta-Wye Connection Lag Example

transformer_ddy_lead30: Linear non-ideal transformer with Delta-Delta-Wye connection, lead 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

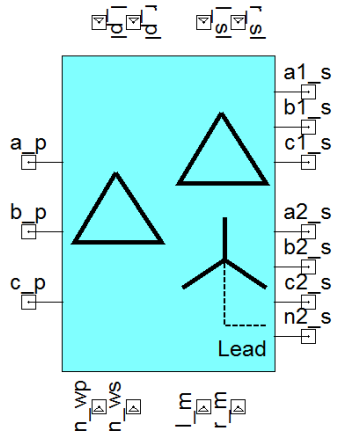

Figure 1. Component symbol

Description

The **transformer_ddy_lead30** represents the behavior of a linear non-ideal three phase transformer with Delta as the primary windings connection, two secondary connections with Delta and Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary wye voltage lead the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
a1_s	Electrical port a1_s, secondary side Delta connection phase A	electrical
b1_s	Electrical port b1_s, secondary side Delta connection phase B	electrical
c1_s	Electrical port c1_s, secondary side Delta connection phase C	electrical
a2_s	Electrical port a2_s, secondary side Wye connection phase A	electrical
b2_s	Electrical port b2_s, secondary side Wye connection phase B	electrical
c2_s	Electrical port c2_s, secondary side Wye connection phase C	electrical
n2_s	Electrical port n2_s, secondary side Wye connection neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary	current	0.0 [A]

	windings		
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Delta-Delta-Wye Connection Lead Example

transformer_dy_lag30: Linear non-ideal transformer with Delta-Wye connection, lag 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

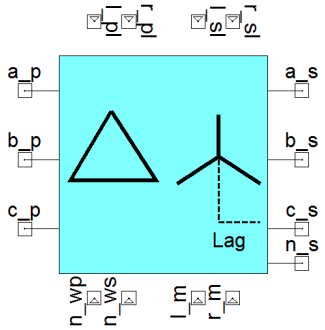

Figure 1. Component symbol

Description

The **transformer_dy_lag30** represents the behavior of a step up linear non-ideal three phase transformer with Delta-Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary voltages lag the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical
n_s	Electrical port n_s, secondary side neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage res-	Input	resistance

	istance.		
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Delta Wye Connection Lag Example

transformer_dy_lead30: Linear non-ideal transformer with Delta-Wye connection, lead 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

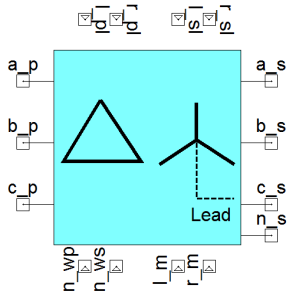

Figure 1. Component symbol

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Description

The **transformer_dy_lead30** represents the behavior of a step up linear non-ideal three phase transformer with Delta-Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary voltages lead the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical
n_s	Electrical port n_s, secondary side neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Delta Wye Connection Lead Example

transformer_yd_lag30: Linear non-ideal transformer with Wye-Delta connection, lag 30 degree

Library: Power System	Modeling Language:	Version Number: Twin

VHDLAMS	VHDL-AMS	Builder 2024.2

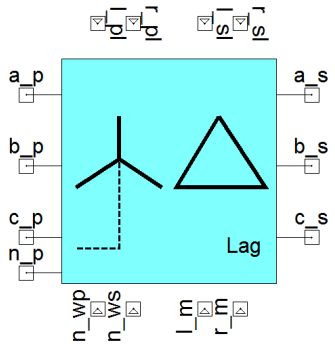

Figure 1. Component symbol

Description

The **transformer_yd_lag30** represents the behavior of a step down linear non-ideal three phase transformer with Wye-Delta connection, includes linear winding leakage and linear core magnetization effects, the secondary voltages lag the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
n_p	Electrical port n_p, primary side neutral	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage res-	Input	resistance

	istance.		
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Wye Delta Connection Lag Example

transformer_yd_lead30: Linear non-ideal transformer with Wye-Delta connection, lead 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

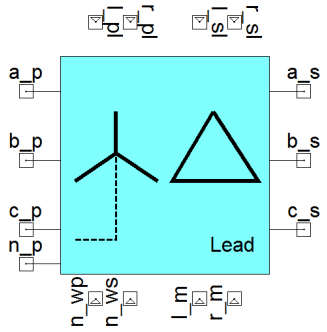

Figure 1. Component symbol

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Description

The **transformer_yd_lead30** represents the behavior of a step down linear non-ideal three phase transformer with Wye-Delta connection, includes linear winding leakage and linear core magnetization effects, the secondary voltages lead the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
n_p	Electrical port n_p, primary side neutral	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Wye Delta Connection Lead Example

transformer_ydy_lag30: Linear non-ideal transformer with Wye-Delta-Wye connection, lag 30 degree

Library: Power System	Modeling Language:	Version Number: Twin

VHDLAMS	VHDL-AMS	Builder 2024.2

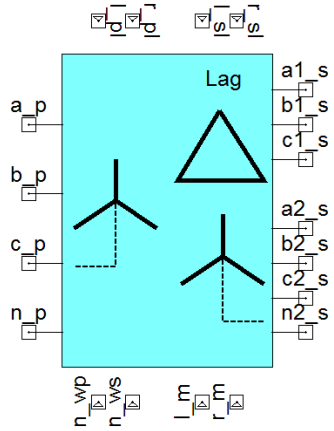

Figure 1. Component symbol

Description

The **transformer_ydy_lag30** represents the behavior of a linear non-ideal three phase transformer with Wye as the primary windings connection, two secondary connections with Delta and Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary delta voltage lag the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
n_p	Electrical port n_p, primary side neutral	electrical
a1_s	Electrical port a1_s, secondary side Delta connection phase A	electrical
b1_s	Electrical port b1_s, secondary side Delta connection phase B	electrical
c1_s	Electrical port c1_s, secondary side Delta connection phase C	electrical
a2_s	Electrical port a2_s, secondary side Wye connection phase A	electrical
b2_s	Electrical port b2_s, secondary side Wye connection phase B	electrical
c2_s	Electrical port c2_s, secondary side Wye connection phase C	electrical
n2_s	Electrical port n2_s, secondary side Wye connection neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]

flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Wye-Delta-Wye Connection Lag Example

transformer_ydy_lead30: Linear non-ideal transformer with Wye-Delta-Wye connection, lead 30 degree

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

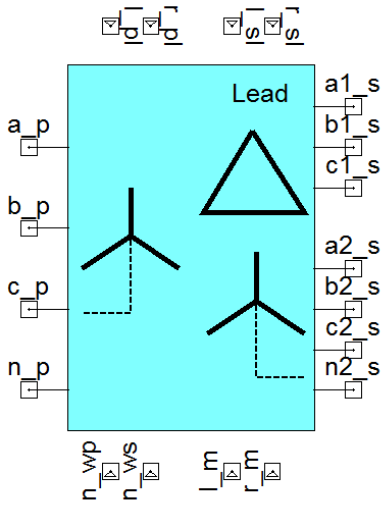

Figure 1. Component symbol

Description

The **transformer_ydy_lead30** represents the behavior of a linear non-ideal three phase transformer with Wye as the primary windings connection, two secondary connections with Delta and Wye connection, includes linear winding leakage and linear core magnetization effects, the secondary delta voltage lead the primary voltages by 30 degrees.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical
b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
n_p	Electrical port n_p, primary side neutral	electrical
a1_s	Electrical port a1_s, secondary side Delta connection phase A	electrical
b1_s	Electrical port b1_s, secondary side Delta connection phase B	electrical
c1_s	Electrical port c1_s, secondary side Delta connection phase C	electrical
a2_s	Electrical port a2_s, secondary side Wye connection phase A	electrical
b2_s	Electrical port b2_s, secondary side Wye connection phase B	electrical
c2_s	Electrical port c2_s, secondary side Wye connection phase C	electrical
n2_s	Electrical port n2_s, secondary side Wye connection neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance
r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Example

Transformer Wye-Delta-Wye Connection Lead Example

transformer_yy: Linear non-ideal transformer with Wye-Wye connection

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

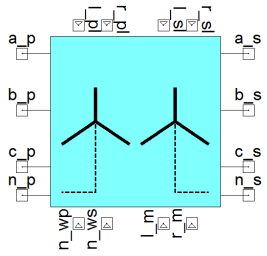

Figure 1. Component symbol

Description

The **transformer_yy** represents the behavior of a linear non-ideal three phase transformer with Wye-Wye connection, includes linear winding leakage and linear core magnetization effects.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_p	Electrical port a_p, primary side phase A	electrical

b_p	Electrical port b_p, primary side phase B	electrical
c_p	Electrical port c_p, primary side phase C	electrical
n_p	Electrical port n_p, primary side neutral	electrical
a_s	Electrical port a_s, secondary side phase A	electrical
b_s	Electrical port b_s, secondary side phase B	electrical
c_s	Electrical port c_s, secondary side phase C	electrical
n_s	Electrical port n_s, secondary side neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
flux0	Initial flux	real	0.0 [Wb]
ilp_0	initial current for leakage inductance on primary windings	current	0.0 [A]
ils_0	initial current for leakage inductance on secondary windings	current	0.0 [A]
im_0	initial current for magnetization inductance	current	0.0 [A]
use_i0	use the initial value or not	boolean	true

Input/Output Quantities

Table 3

Name	Description [Unit]	Direction	Data Type
r_pl	primary winding leakage resistance.	Input	resistance
l_pl	primary winding leakage inductance.	Input	inductance

r_sl	secondary winding leakage resistance.	Input	resistance
l_sl	secondary winding leakage resistance.	Input	resistance
r_m	magnetization resistance for the primary winding	input	resistance
l_m	magnetization inductance for the primary winding	Input	inductance
n_wp	number of winding turns for primary windings	input	real
n_ws	number of winding turns for secondary windings	input	real

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Transformer Wye-Wye Connection Example

Transmission Line

The Transmission Line sublibrary consists of single phase and balanced, transpose three phase low frequency transmission line models for power systems, and it contains:

- Single phase low frequency short transmission line
- Balanced and transpose three phase low frequency short transmission line
- Single phase low frequency medium transmission line, nominal PI
- Single phase low frequency medium transmission line, nominal T
- Balanced and transpose three phase low frequency medium transmission line, nominal PI
- Balanced and transpose three phase low frequency medium transmission line, nominal T
- Single phase low frequency transmission line segment for long transmission line
- Single phase low frequency long transmission line with distributed segments
- Three phase low frequency transmission line segment for long transmission line
- Three phase low frequency long transmission line with distributed segments

tlsl: Single phase low frequency long transmission line with distributed segments

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

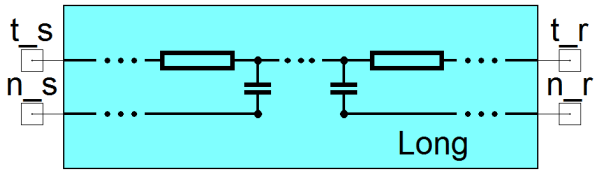

Figure 1. Component symbol

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• Netlist Syntax

• Conservative Pins

• Parameters

• Input/Output Quantities

• Example

Description

The **tlsl** represents the behavior of single phase low frequency long transmission line model with length usually longer than 150km and the line voltage is high (>100kV). Due to length and voltage of the line, lumped parameters are no longer proper for the performance calculations. The line constants will be considered as uniformly distributed throughout the length of the line.

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Table 1

Name	Port/Terminal description	Nature/Data type
t_s	Electrical port t_s, the sending terminal.	electrical
t_r	Electrical port t_r, the receiving terminal	electrical
n_s	Electrical port n_s, the neutral.	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the trans-mission line	real	200000.0 [m]
n	number of segments in the transmission line	integer	100

r_tl	resistance per length	real	2.0e-4 [Ohm/m]
l_tl	inductance per length	real	2.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
g_tl	conductance per length	real	2.0e-5 [S/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Long Single Phase Example

tlsl_s: Single phase low frequency transmission line segment for long transmission line

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

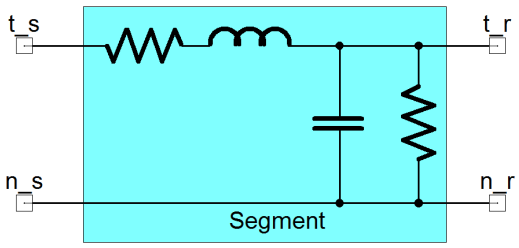

Figure 1. Component symbol

Description

The **tlsl_s** represents the behavior of single phase low frequency transmission line segment model for the long transmission line with length usually longer than 150km and the line voltage is high (>100kV). Due to length and voltage of the line, lumped parameters are no longer proper for the performance calculations. The line constants will be considered as uniformly distributed throughout the length of the line.

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Table 1

Name	Port/Terminal description	Nature/Data type
t_s	Electrical port t_s, the sending terminal.	electrical
t_r	Electrical port t_r, the receiving terminal	electrical
n_s	Electrical port n_s, the neutral.	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]

len	length of the transmission line	real	50.0 [m]
r_tl	resistance per length	real	2.0e-4 [Ohm/m]
l_tl	inductance per length	real	2.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
g_tl	conductance per length	real	2.0e-5 [S/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Long Single Phase Segment Example

tlsm_pi: Single phase low frequency medium transmission line, nominal PI

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

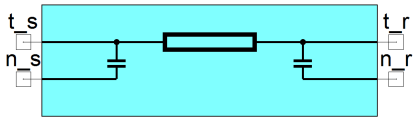

Figure 1. Component symbol

• Example

Description

The **tlsm_pi** represents the behavior of single phase low frequency transmission line model (nominal PI, the capacitance from line to neutral is divided into two halves, one half being lumped at the sending end and the other half at the receiving end) with length between 50 km and 150km and the line voltage is moderatly high (>20kV and <100kV). It is usually considered as a medium transmission line. Due to sufficient length and voltage of the line, the capacitance effects are taken into account. This is a lumped model.

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Table 1

Name	Port/Terminal description	Nature/Data type
t_s	Electrical port t_s, the sending terminal.	electrical
t_r	Electrical port t_r, the receiving terminal	electrical
n_s	Electrical port n_s, the neutral.	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the trans-	real	50000.0 [m]

	mission line		
r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Medium Single Phase PI Example

tlsm_t: Single phase low frequency medium transmission line, nominal T

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

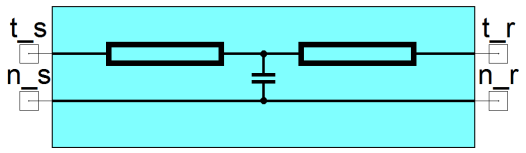

Figure 1. Component symbol

Description

The **tlsm_t** represents the behavior of single phase low frequency transmission line model (nominal T, the whole line capacitance is assumed to be concentrated at the middle point of the line and half of the line resistance and inductance are lumped on its either side) with length between 50 km and 150km and the line voltage is moderatly high (>20kV and <100kV). It is usually considered as a medium transmission line. Due to sufficient length and voltage of the line, the capacitance effects are taken into account. This is a lumped model.

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Table 1

Name	Port/Terminal description	Nature/Data type
t_s	Electrical port t_s, the sending terminal.	electrical
t_r	Electrical port t_r, the receiving terminal	electrical
n_s	Electrical port n_s, the neutral.	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the transmission line	real	50000.0 [m]

r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

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Example

Transmission Line Medium Single Phase T Example

tlss: Single phase low frequency short transmission line

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

Description

The **tlss** represents the behavior of single phase low frequency transmission line model with length less than 50 km and the line voltage is comparatively low (< 20 kV). It is usually considered as a short transmission line. Due to the smaller length and lower voltage, the capacitance effects are small hence can be neglected. Therefore, while studying the performance of a short transmission line, only lumped resistance and inductance of the line are taken into account.

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Table 1

Name	Port/Terminal description	Nature/Data type
t_s	Electrical port t_s, the sending terminal.	electrical
t_r	Electrical port t_r, the receiving terminal	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the transmission line	real	50000.0 [m]
r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
i_0	initial current for transmission line	current	0.0 [A]

use_i0	use the initial current values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Short Single Phase Example

tltl: Three phase low frequency transmission line for long transmission line

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

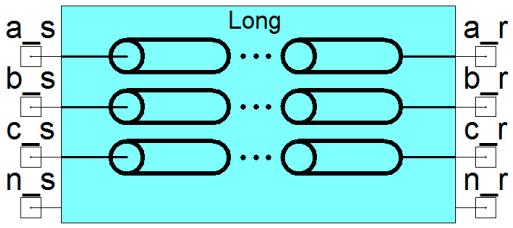

Figure 1. Component symbol

Description

The **tltl** represents the behavior of three phase low frequency long transmission line model with length usually longer than 150km and the line voltage is high (>100kV). Due to length and voltage of the line, lumped parameters are no longer proper for the performance calculations. The line constants will be considered as uniformly distributed throughout the length of the line.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_s	Electrical port a_s, the sending terminal phase A.	electrical
b_s	Electrical port b_s, the sending terminal phase B.	electrical
c_s	Electrical port c_s, the sending terminal phase C.	electrical
a_r	Electrical port a_r, the receiving terminal phase A	electrical
b_r	Electrical port b_r, the receiving terminal phase B	electrical
c_r	Electrical port c_r, the receiving terminal phase C	electrical
n_s	Electrical port n_s, the neutral	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the trans-	real	200000.0 [m]

	mission line		
n	number of segments in the transmission line	integer	100
r_a	resistance per length for phase A	real	2.0e-4 [Ohm/m]
l_a	inductance per length for phase A	real	2.0e-6 [H/m]
c_a0	capacitance per length between phase A and neutral	real	8.6e-12 [F/m]
g_a0	conductance per length between phase A and neutral	real	2.0e-5 [S/m]
r_b	resistance per length for phase B	real	2.0e-4 [Ohm/m]
l_b	inductance per length for phase B	real	2.0e-6 [H/m]
c_b0	capacitance per length between phase B and neutral	real	8.6e-12 [F/m]
g_b0	conductance per length between phase B and neutral	real	2.0e-5 [S/m]
r_c	resistance per length for phase C	real	2.0e-4 [Ohm/m]
l_c	inductance per length for phase C	real	2.0e-6 [H/m]
c_c0	capacitance per length between phase C and neutral	real	8.6e-12 [F/m]
g_c0	conductance per length between phase C and neutral	real	2.0e-5 [S/m]
r_0	resistance per length for neutral	real	2.0e-4 [Ohm/m]
l_0	inductance per length for neutral	real	2.0e-6 [H/m]
c_ab	capacitance per length between phase a and b	real	8.6e-12 [F/m]
g_ab	conductance per length between phase a and b	real	2.0e-5 [S/m]
c_bc	capacitance per length between phase b and c	real	8.6e-12 [F/m]
g_bc	conductance per length between phase b and c	real	2.0e-5 [S/m]
c_ca	capacitance per length between phase c and a	real	8.6e-12 [F/m]

g_ca	conductance per length between phase c and a	real	2.0e-5 [S/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

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Example

Transmission Line Long Three Phase Example

tltl_s: Three phase low frequency transmission line segment for long transmission line

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

Description

The **tltl_s** represents the behavior of three phase low frequency transmission line segment model for the long transmission line with length usually longer than 150km and the line voltage is high (>100kV). Due to length and voltage of the line, lumped parameters are no longer proper for the performance calculations. The line constants will be considered as uniformly distributed throughout the length of the line.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_s	Electrical port a_s, the sending terminal phase A.	electrical
b_s	Electrical port b_s, the sending terminal phase B.	electrical
c_s	Electrical port c_s, the sending terminal phase C.	electrical
a_r	Electrical port a_r, the receiving terminal phase A	electrical
b_r	Electrical port b_r, the receiving terminal phase B	electrical
c_r	Electrical port c_r, the receiving terminal phase C	electrical
n_s	Electrical port n_s, the neutral	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the trans-mission line	real	50.0 [m]
r_a	resistance per length for phase A	real	2.0e-4 [Ohm/m]
l_a	inductance per length for phase A	real	2.0e-6 [H/m]
c_a0	capacitance per length between phase A and neutral	real	8.6e-12 [F/m]
g_a0	conductance per length between phase A and neutral	real	2.0e-5 [S/m]
r_b	resistance per length for phase B	real	2.0e-4 [Ohm/m]
l_b	inductance per length for phase B	real	2.0e-6 [H/m]
c_b0	capacitance per length between phase B and neutral	real	8.6e-12 [F/m]
g_b0	conductance per length between phase B and neutral	real	2.0e-5 [S/m]
r_c	resistance per length for phase C	real	2.0e-4 [Ohm/m]
l_c	inductance per length for phase C	real	2.0e-6 [H/m]
c_c0	capacitance per length between phase C and neutral	real	8.6e-12 [F/m]
g_c0	conductance per length between phase C and neutral	real	2.0e-5 [S/m]
r_0	resistance per length for neutral	real	2.0e-4 [Ohm/m]
l_0	inductance per length for neutral	real	2.0e-6 [H/m]
c_ab	capacitance per length	real	8.6e-12 [F/m]

	between phase a and b		
g_ab	conductance per length between phase a and b	real	2.0e-5 [S/m]
c_bc	capacitance per length between phase b and c	real	8.6e-12 [F/m]
g_bc	conductance per length between phase b and c	real	2.0e-5 [S/m]
c_ca	capacitance per length between phase c and a	real	8.6e-12 [F/m]
g_ca	conductance per length between phase c and a	real	2.0e-5 [S/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

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Example

Transmission Line Long Three Phase Segment Example

tltm_pi: Balanced and transpose three phase low frequency medium transmission line, nominal PI

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

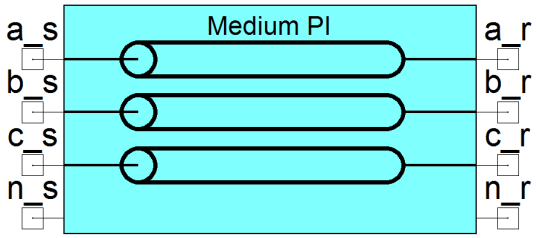

Figure 1. Component symbol

- Description
- Assumptions and Limitations

Description

The **tltm_pi** represents the behavior of balanced and transpose three phase low frequency transmission line model (nominal PI, the capacitance from line to neutral is divided into two halves, one half being lumped at the sending end and the other half at the receiving end) with length between 50 km and 150km and the line voltage is moderatly high (>20kV and <100kV). It is usually considered as a medium transmission line. Due to sufficient length and voltage of the line, the capacitance effects are taken into account. This is a lumped model.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_s	Electrical port a_s, the sending terminal phase A.	electrical
b_s	Electrical port b_s, the sending terminal phase B.	electrical
c_s	Electrical port c_s, the sending terminal phase C.	electrical
a_r	Electrical port a_r, the receiving terminal phase A	electrical
b_r	Electrical port b_r, the receiving terminal phase	electrical

	B	
c_r	Electrical port c_r, the receiving terminal phase C	electrical
n_s	Electrical port n_s, the neutral	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the transmission line	real	50000.0 [m]
r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Medium Three Phase PI Example

tltm_t: Balanced and transpose three phase low frequency medium transmission line, nominal T

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

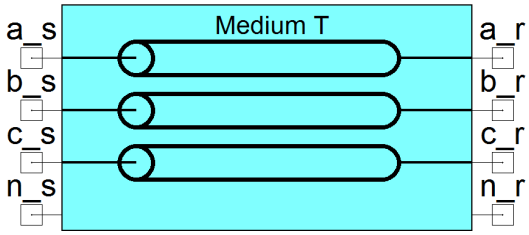

Figure 1. Component symbol

Description

The **tltm_t** represents the behavior of balanced and transpose three phase low frequency transmission line model (nominal T, the whole line capacitance is assumed to be concentrated at the middle point of the line and half of the line resistance and inductance are lumped on its either side) with length between 50 km and 150km and the line voltage is moderatly high (>20kV and <100kV). It is usually considered as a medium transmission line. Due to sufficient length and voltage of the line, the capacitance effects are taken into account. This is a lumped model.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_s	Electrical port a_s, the sending terminal phase A.	electrical
b_s	Electrical port b_s, the sending terminal phase B.	electrical
c_s	Electrical port c_s, the sending terminal phase C.	electrical
a_r	Electrical port a_r, the receiving terminal phase A	electrical
b_r	Electrical port b_r, the receiving terminal phase B	electrical
c_r	Electrical port c_r, the receiving terminal phase C	electrical
n_s	Electrical port n_s, the neutral	electrical
n_r	Electrical port n_r, the neutral	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

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Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the transmission line	real	50000.0 [m]
r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
c_tl	capacitance per length	real	8.6e-12 [F/m]
i_0	initial current for transmission line	current	0.0 [A]
use_i0	use the initial current values or not	Boolean	true
v_0	initial voltage for transmission line	voltage	0.0 [V]
use_v0	use the initial voltage values or not	Boolean	true

Input/Output Quantities

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Example

Transmission Line Medium Three Phase T Example

tlts: Balanced and transpose three phase low frequency short transmission line

Library: Power System VHDLAMS	Modeling Language: VHDL-AMS	Version Number: Twin Builder 2024.2

Figure 1. Component symbol

Description

The **tlts** represents the behavior of balanced and transpose three phase low frequency transmission line model with length less than 50 km and the line voltage is comparatively low (< 20 kV). It is usually considered as a short transmission line. Due to the smaller length and lower voltage, the capacitance effects are small hence can be neglected. Therefore, while studying the performance of a short transmission line, only lumped resistance and inductance of the line are taken into account.

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Table 1

Name	Port/Terminal description	Nature/Data type
a_s	Electrical port a_s, the sending terminal phase A.	electrical
b_s	Electrical port b_s, the sending terminal phase B.	electrical
c_s	Electrical port c_s, the sending terminal phase C.	electrical
a_r	Electrical port a_r, the receiving terminal phase A	electrical
b_r	Electrical port b_r, the receiving terminal phase B	electrical
c_r	Electrical port c_r, the receiving terminal phase C	electrical

Note: Terminal set to No Action when unconnected. Terminal may remain unconnected without generating an error.

Parameters

Top

Table 2

Name	Description	Data Type	Default Value [Unit]
len	length of the trans-mission line	real	50000.0 [m]
r_tl	resistance per length	real	1.0e-5 [Ohm/m]
l_tl	inductance per length	real	1.0e-6 [H/m]
i_0	initial current for trans-mission line	current	0.0 [A]
use_i0	use the initial current val-	Boolean	true

	ues or not		

Input/Output Quantities

Top

Example

Transmission Line Short Three Phase Example

AC Sources Example

Description

The AC Sources schematic is shown in Figure 1.

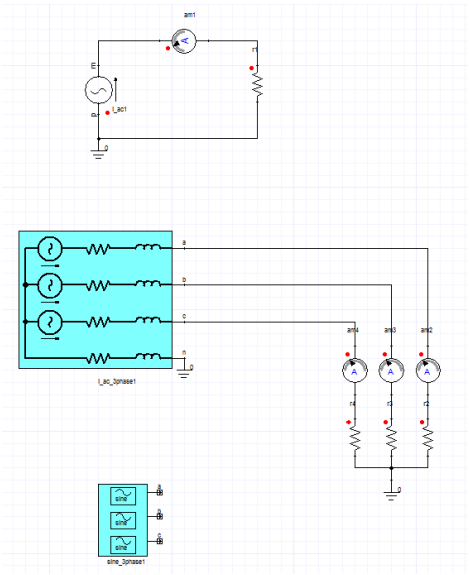


Figure 1: AC SourcesSchematic

The system contains the i_ac, i_ac_3phase and sine_3phasemodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofAC source components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The AC current sourceresult is shown in Figure 2.

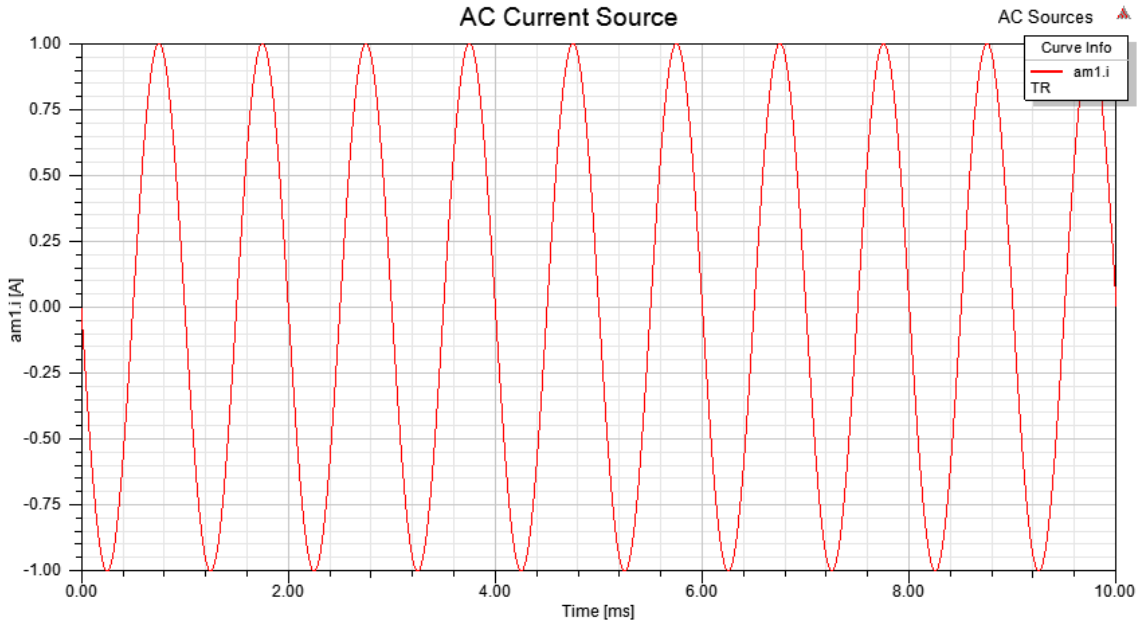


Figure 2: AC Current Source

The 3 phase AC current source result is shown in Figure 3.

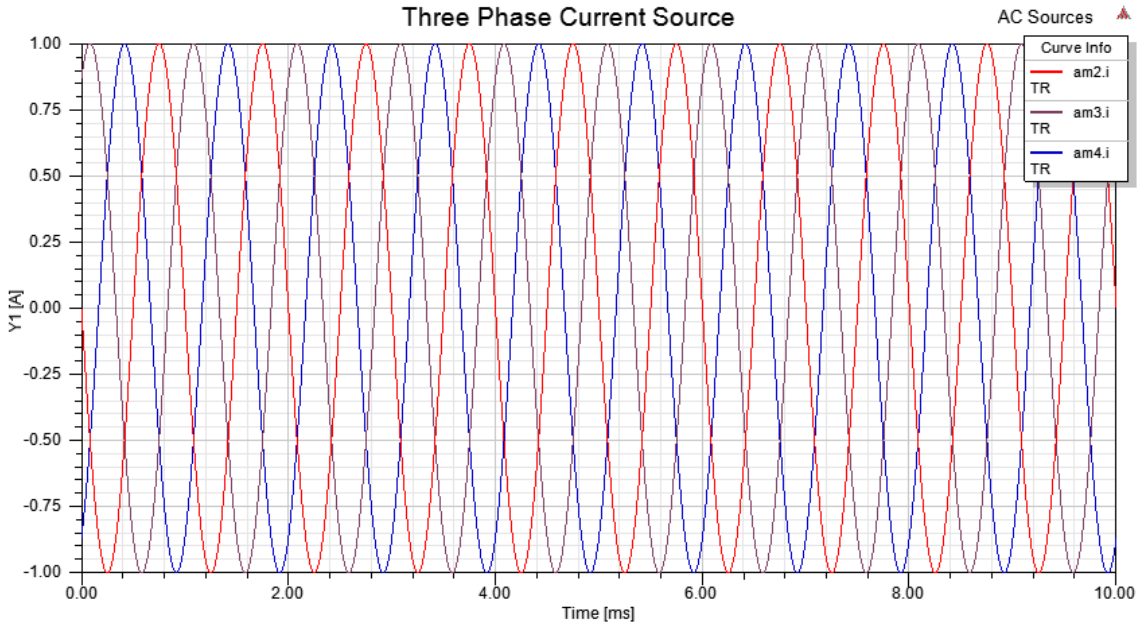


Figure 3: Three Phase AC Current Source

The 3 phase sine wave result isshown in Figure 4.

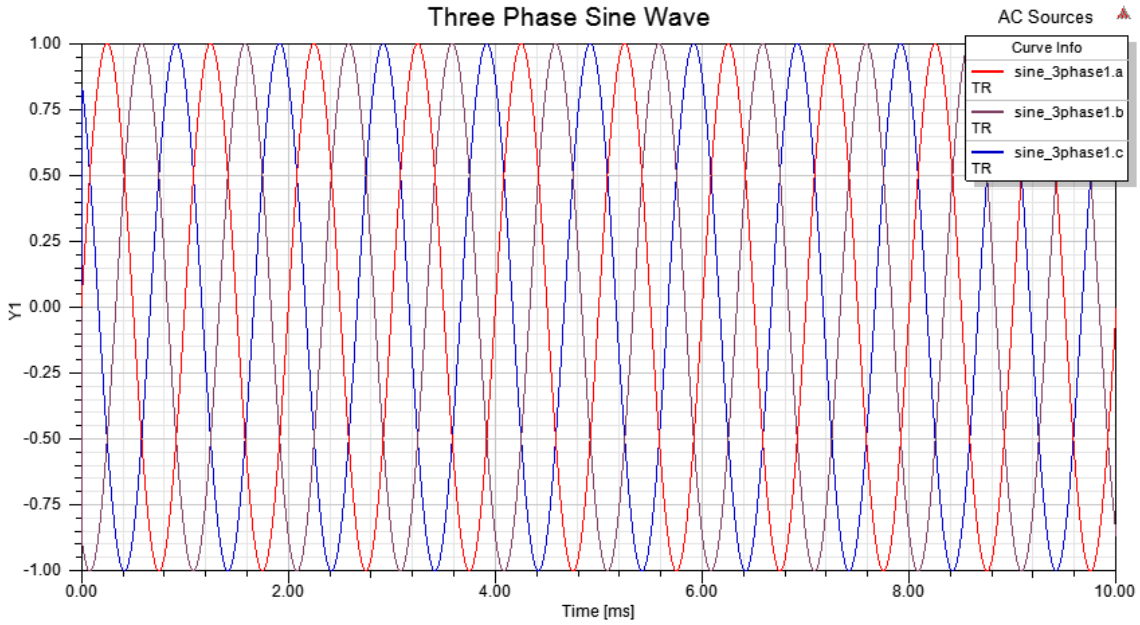


Figure 4: Three Phase Sine Wave Generator

Controlled Sources Example

Description

The Controlled Sources schematic is shown in Figure 1.

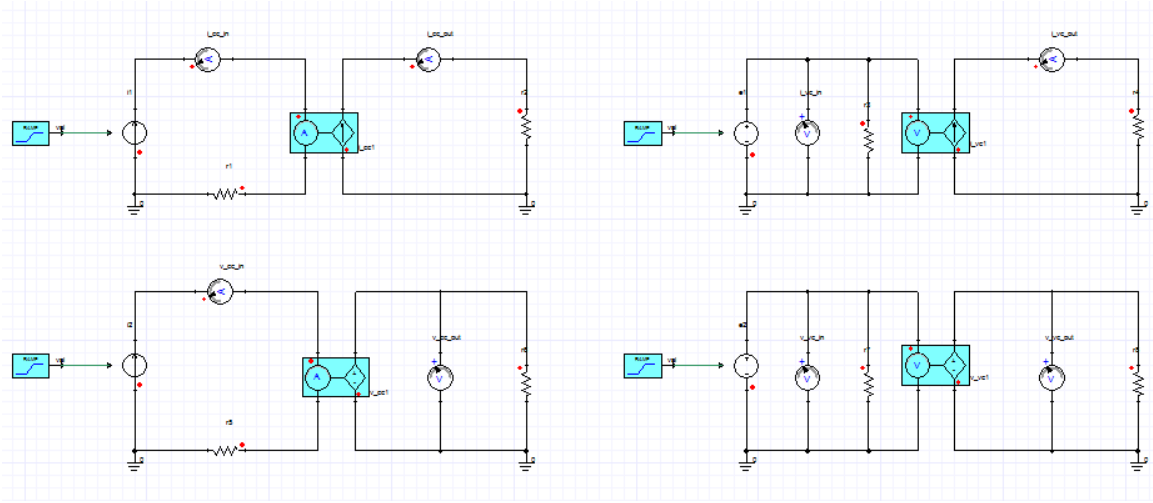


Figure 1: Controlled SourcesSchematic

The system contains thei_cc, i_vc, v_cc and v_vc models from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofcontrolled source components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The current controlled current sourceresult is shown in Figure 2.

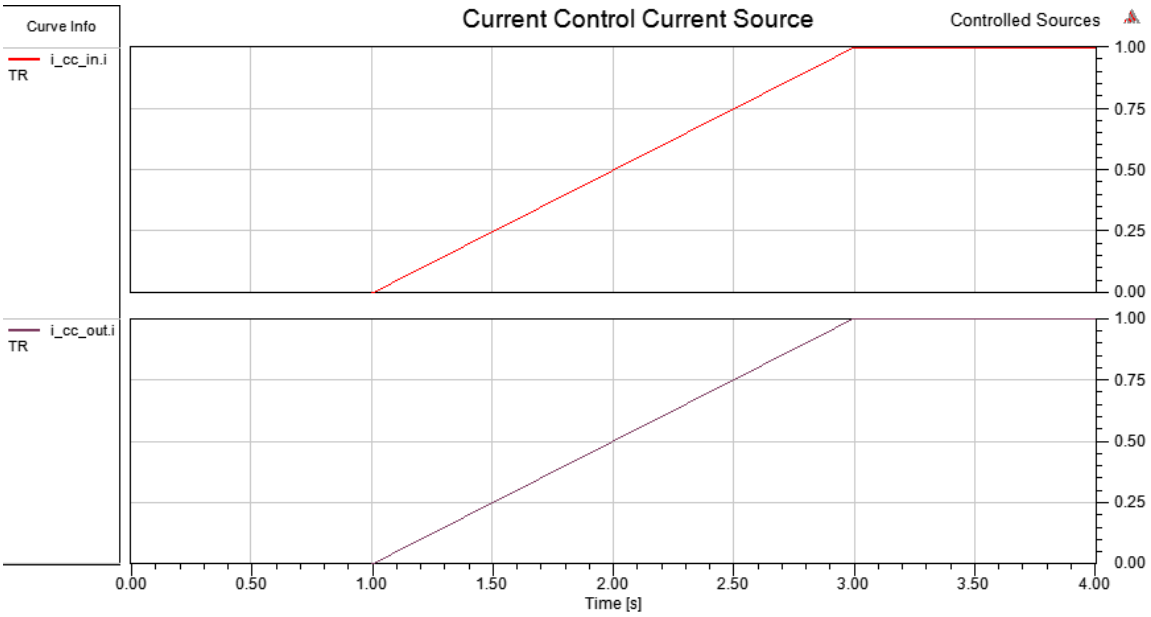


Figure 2: Current Controlled Current Source

The voltage controlled current source result is shown in Figure 3.

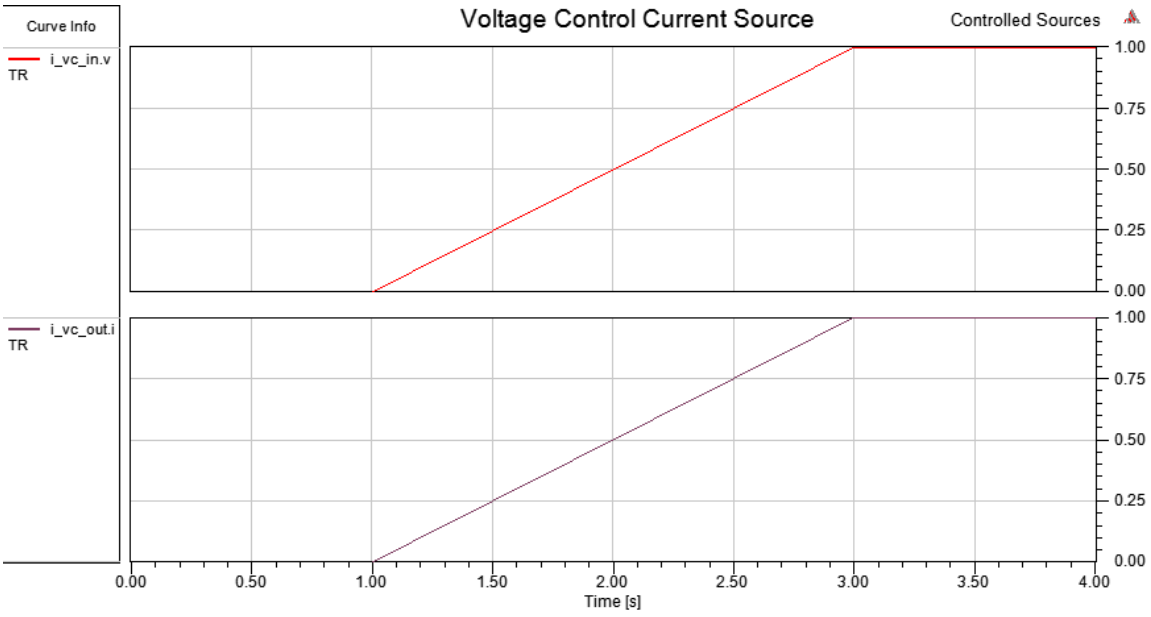


Figure 3: Voltage Controlled Current Source

The current controlled voltage source result isshown in Figure 4.

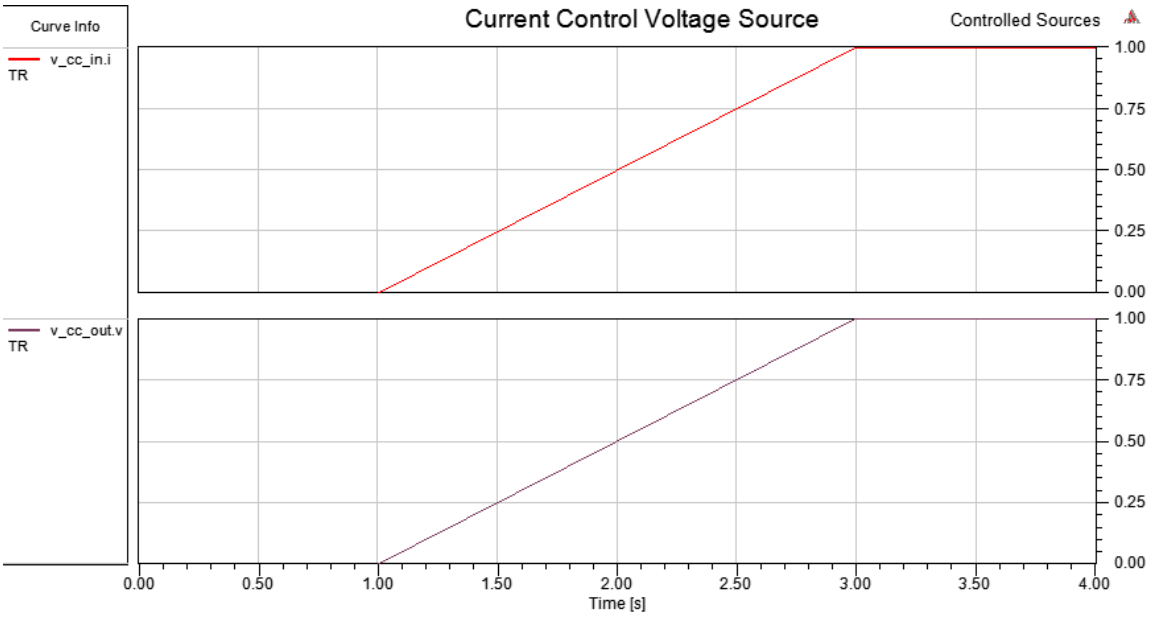


Figure 4: Current Controlled Voltage Source

The voltage controlled voltage source result is shown in Figure 5.

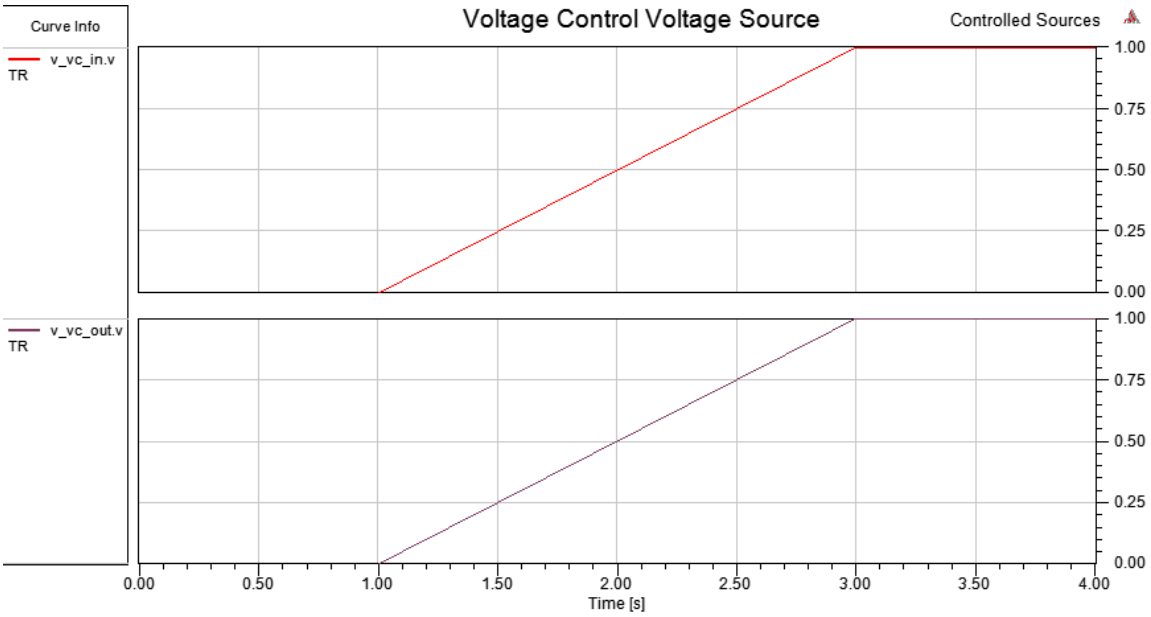


Figure 5: Voltage Controlled Voltage Source

Frequency Dependent Elements Example

Description

The frequency dependent elements schematic is shown in Figure 1.

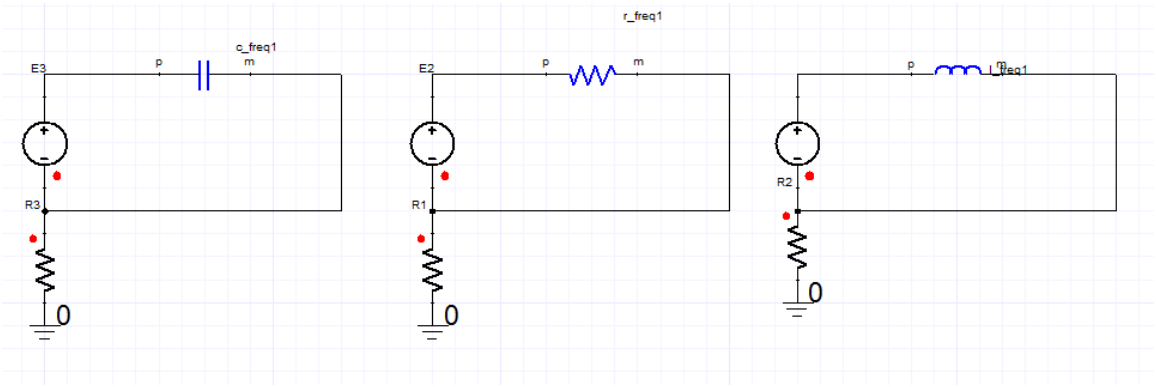


Figure 1: Frequency Dependent ElementsSchematic

The system contains the c_freq, r_freq and l_freq from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage of frequency dependent RLC components from Power System VHDL-AMS library. Results are shown below.

Simulation Results

The frequency response of c_freq is shown in Figure 2.

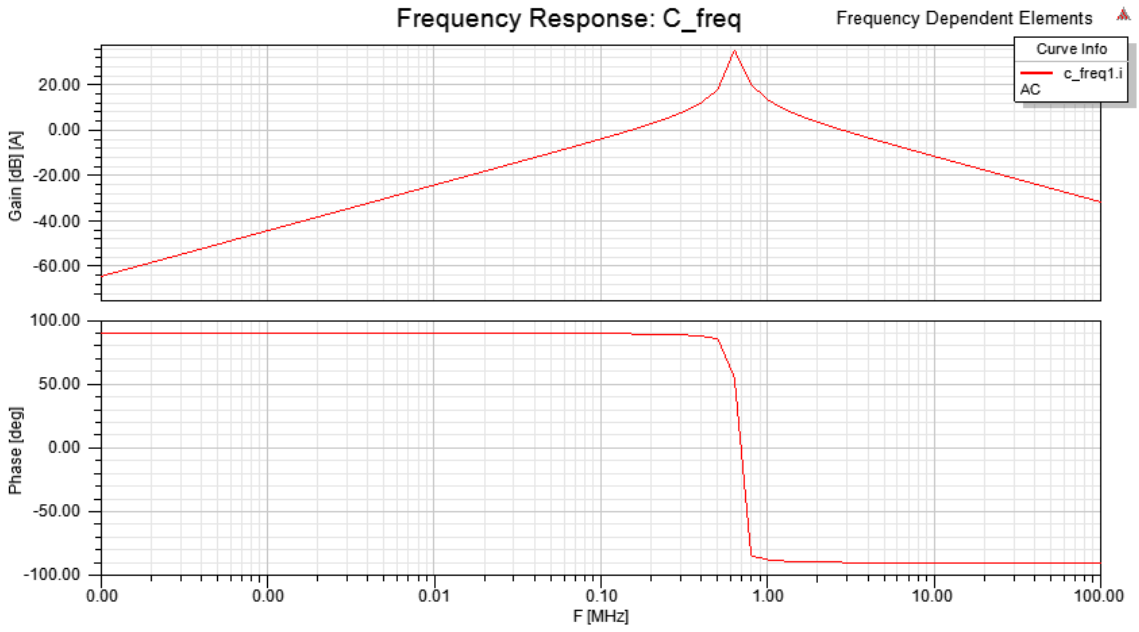


Figure 2: Frequency Response: c_freq

The frequency response of l_freq is shown in Figure 3.

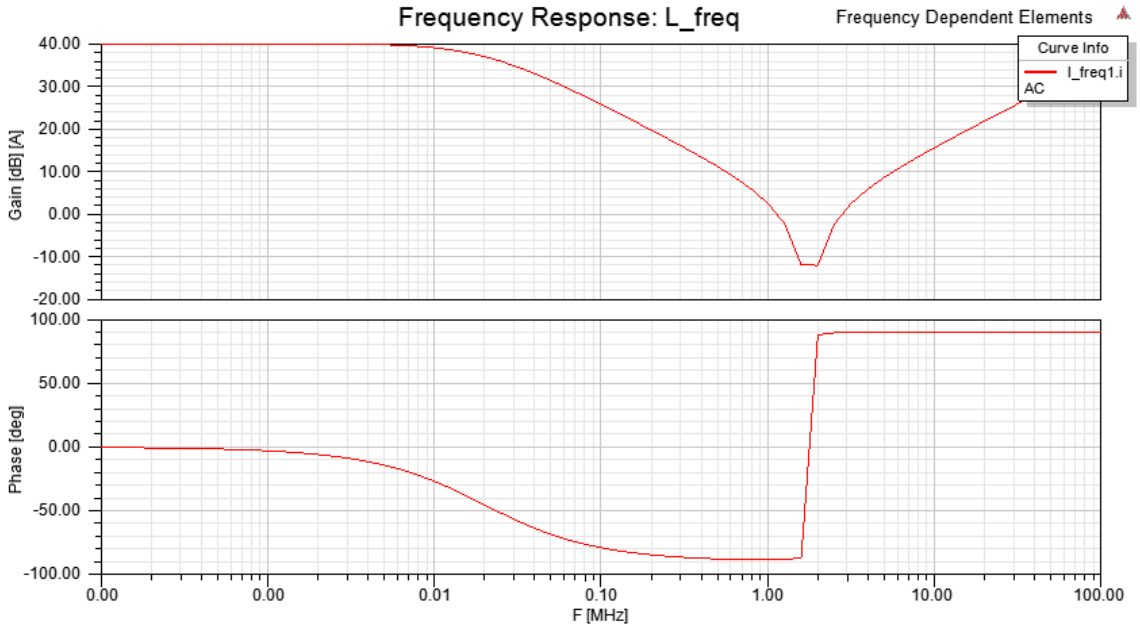


Figure 3: Frequency Response: l_freq

The frequency response of r_freq is shown in Figure 4.

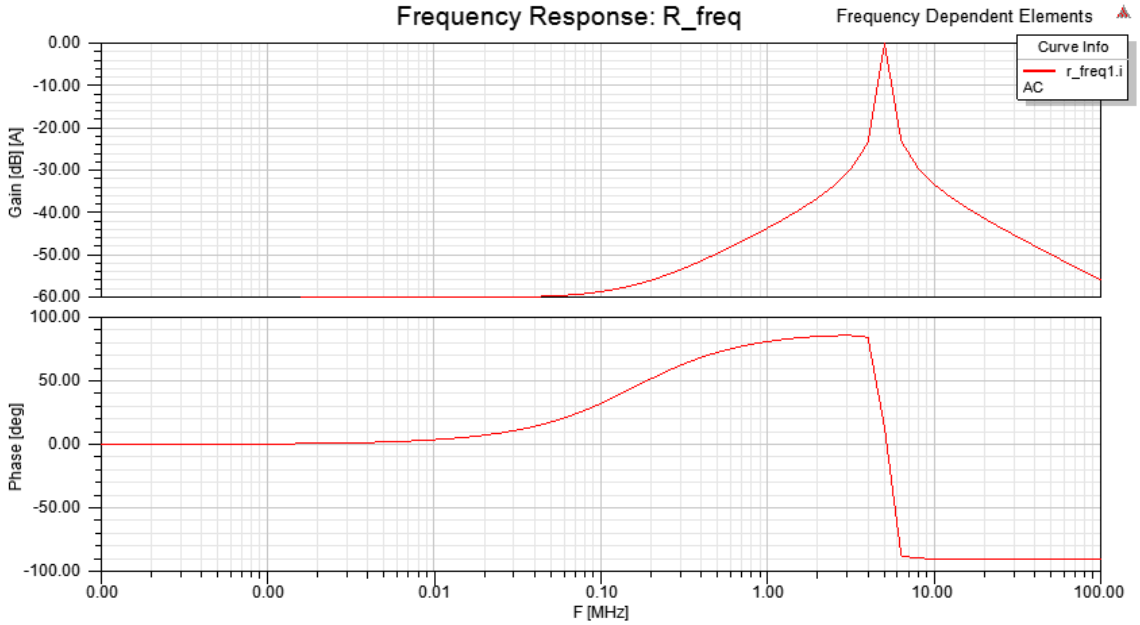


Figure 4: Frequency Response: r_freq

Gyrator Example

Description

The Gyrator schematic is shown in Figure 1.

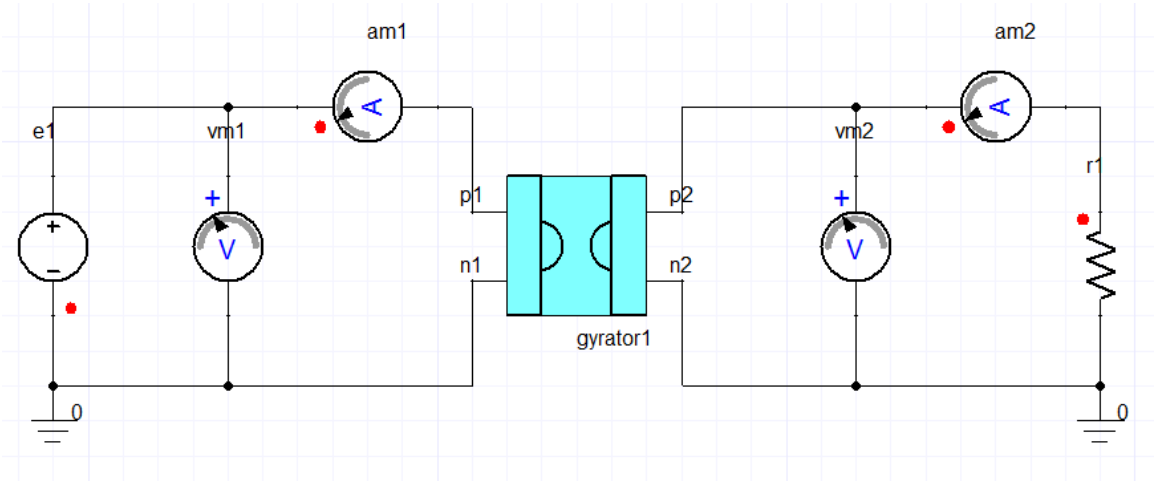


Figure 1: GyratorSchematic

The system contains thegyrator model from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofgyrator model in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The voltage comparison is shown in Figure 2.

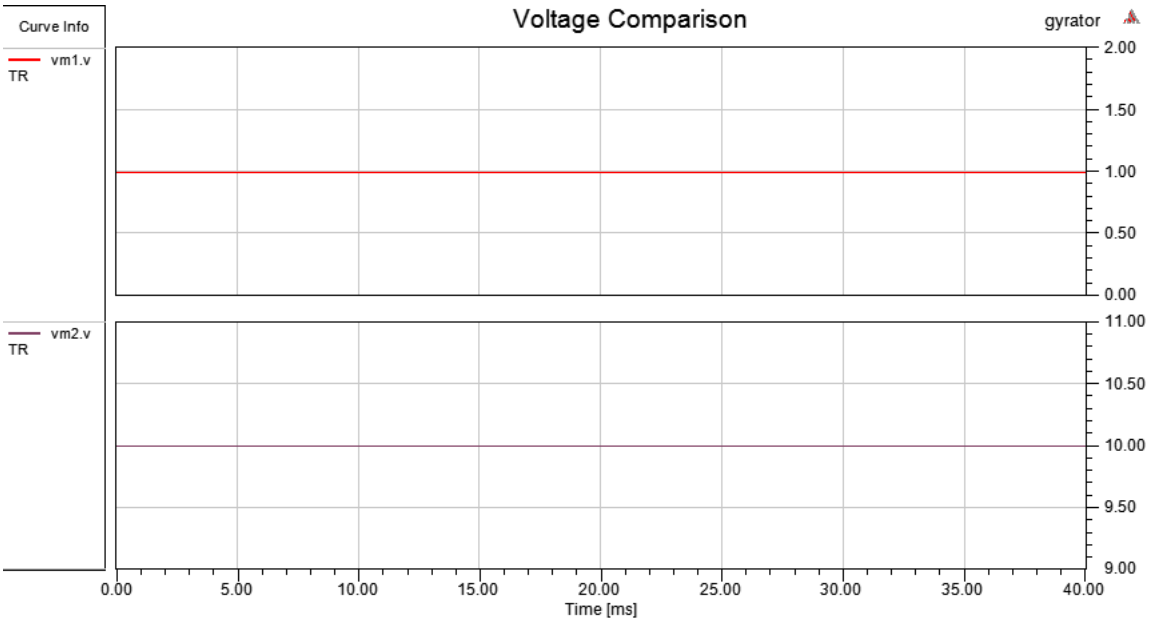


Figure 2: Voltage Comparison

The current comparisonis shown in Figure 3.

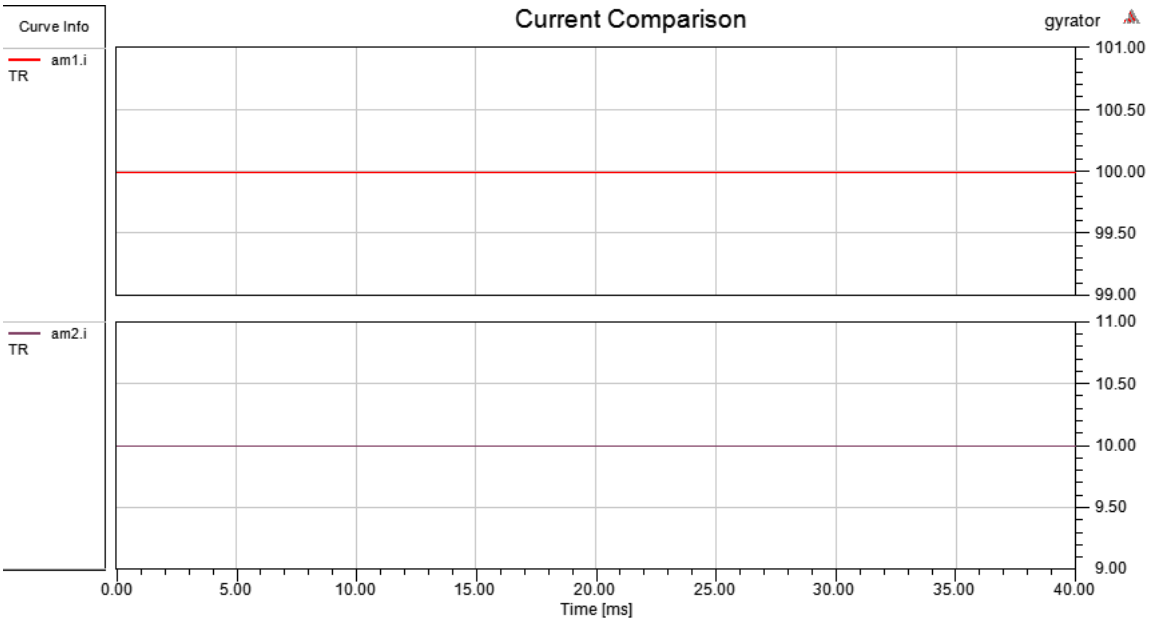


Figure 3: Current Comparison

Ideal Transformer Example

Description

The Ideal Transformer schematic is shown in Figure 1.

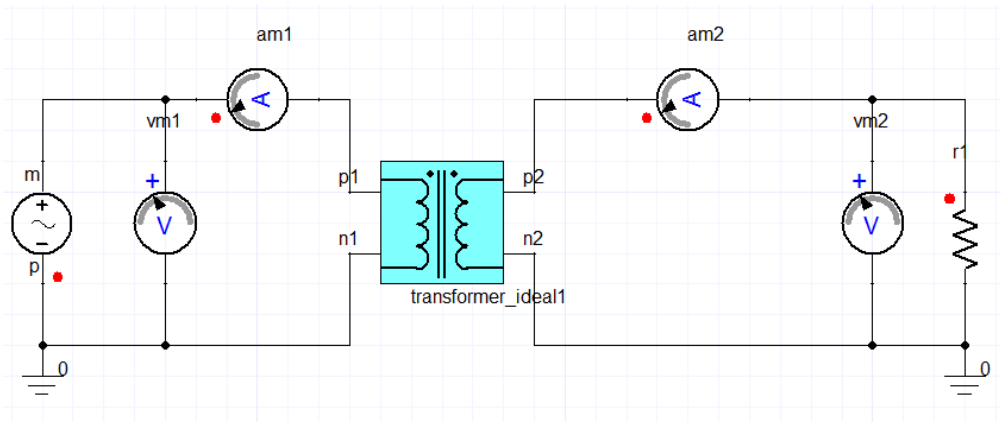


Figure 1: Ideal TransformerSchematic

The system contains thetransformer_idealmodel from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofideal transformer component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The voltage comparison is shown in Figure 2.

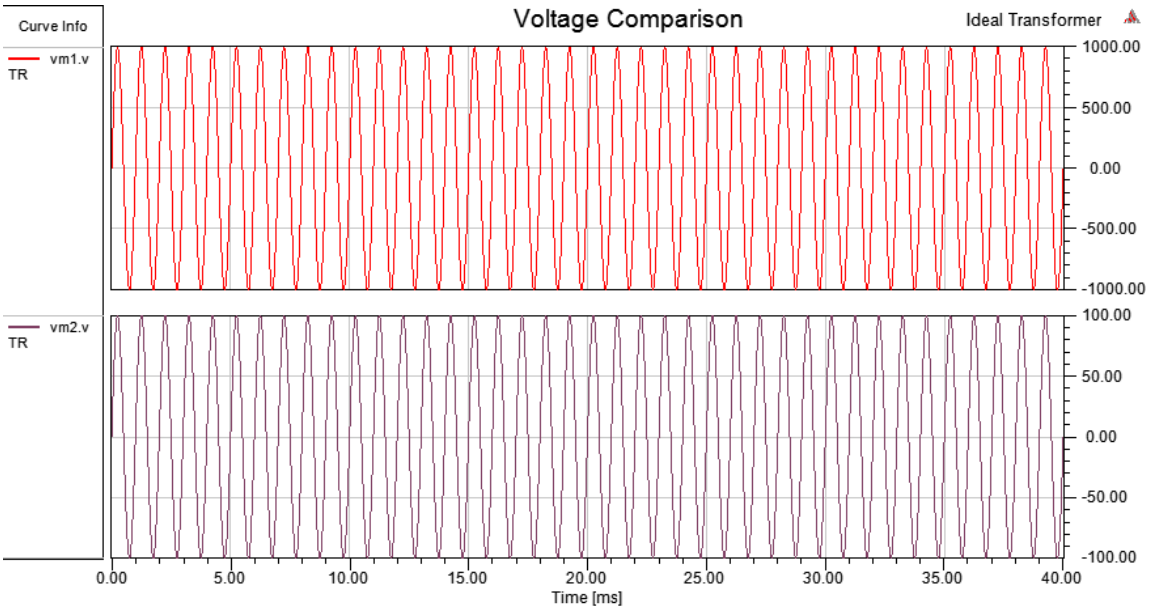


Figure 2: Voltage Comparison

The current comparison is shown in Figure 3.

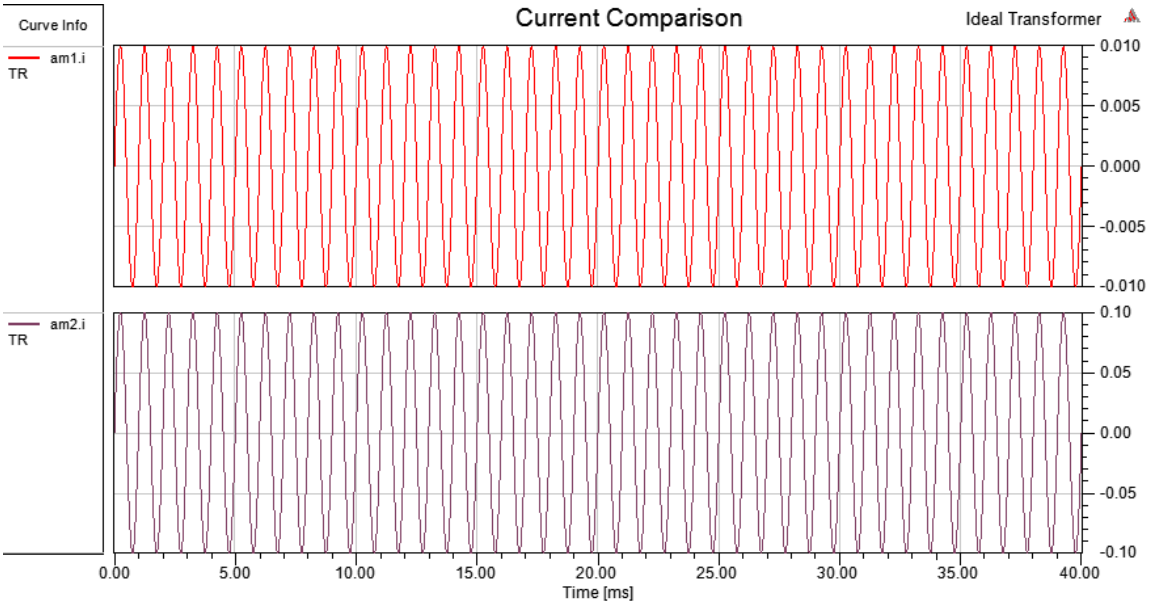


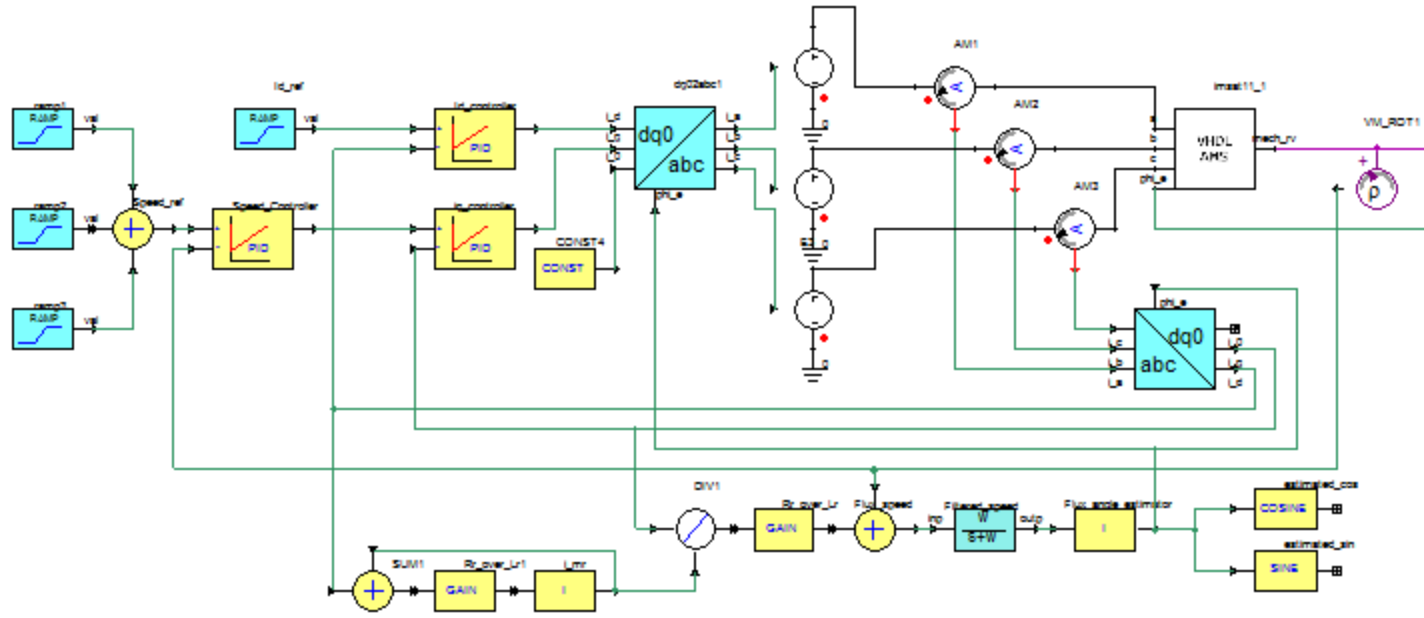
Figure 3: Current Comparison

Induction Motor Speed Control Example

Description

This example shows a field-oriented controller with flux observer to control the speed of a 3-phase induction motor.

Induction motor operates by running 3-phase AC voltage source in the stator to create rotating magnetic field, which induces eddy current in the shorted rotor to produces torque. Field-oriented control is a control method in which the currents in the stator are measured in a rotational orthogonal coordinate system (called d-q frame), which rotates in the same speed as the rotating magnetic field. The currents in the stator can then be separated into part that is parallel to the rotating magnetic field and part that is perpendicular to the rotating magnetic field. The advantage of such transformation is that the AC current can be converted into non-periodic DC values in the d-q plane. Thus, it is much more convenient to control the speed of motor by controlling the DC current values in these two directions. For more information about the coordinate transformation and field-oriented control, please read reference [1].



The system schematic contains the following:

Field-oriented control is implemented according to [1], it consists an outer loop motor speed controller, and inner loop current controllers on d and q axes.

To achieve the field-synchronous d-q frame, a **flux observer** is implemented according to [2], in order to estimate flux angle of the induction motor. The estimated flux angle is used by abc-to-dq transform and inverse transform blocks.

The **induction motor** under control is an equivalent circuit model written in VHDL-AMS. Flux saturation effect is modeled by a 1D lookup table of Flux (lambda) corresponds to magnetizing current (im).

Three ramp changes are used as reference speed signal to demonstrate the performance of this motor controller:

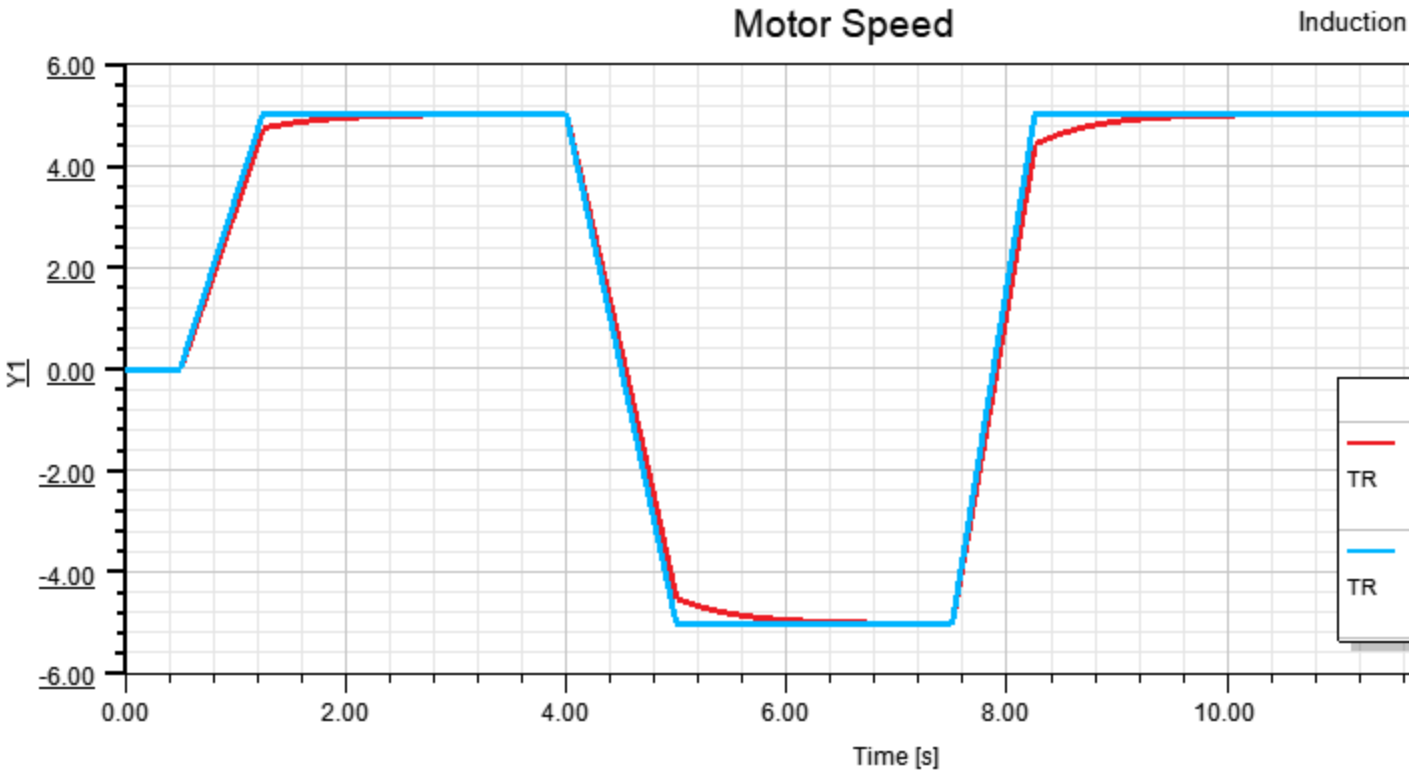
Ramp up at t = 0.5s, from 0 to 5 rad/s, within 0.75 sec

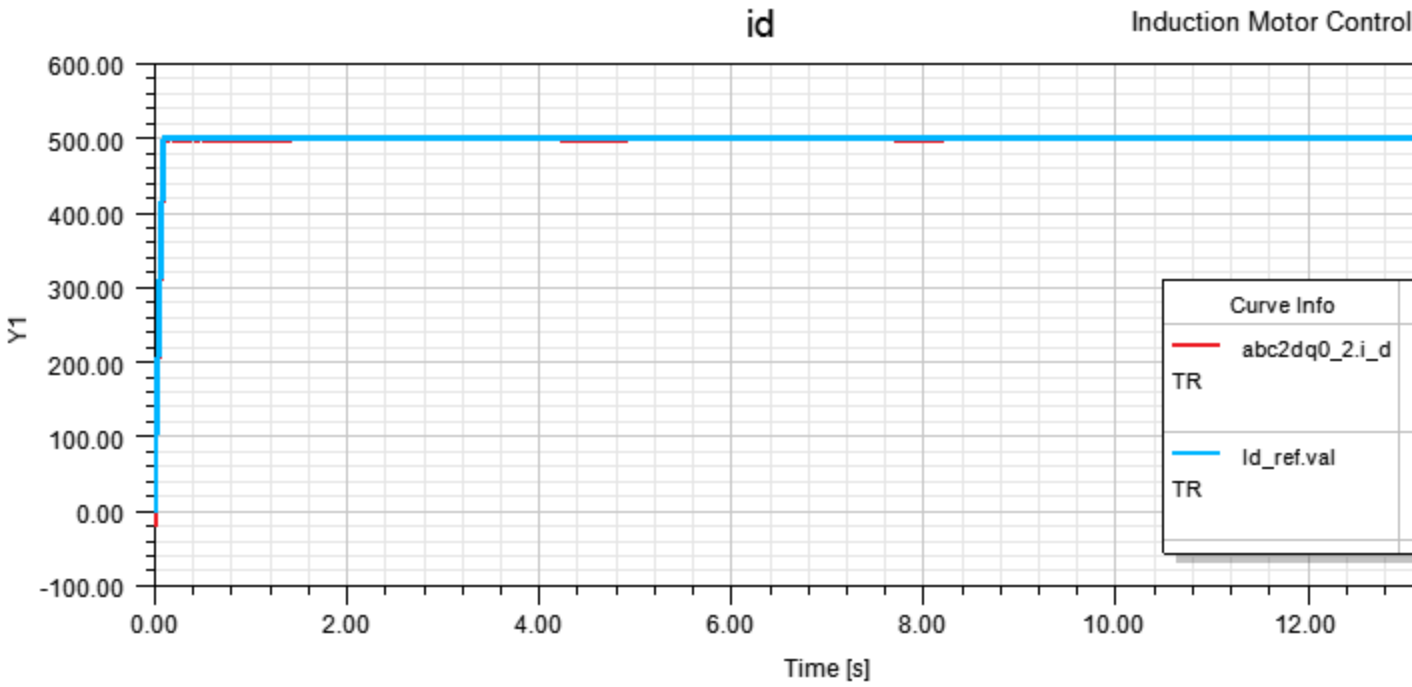
Ramp down at t = 4s, from 5 to -5 rad/s, within 1.0 sec

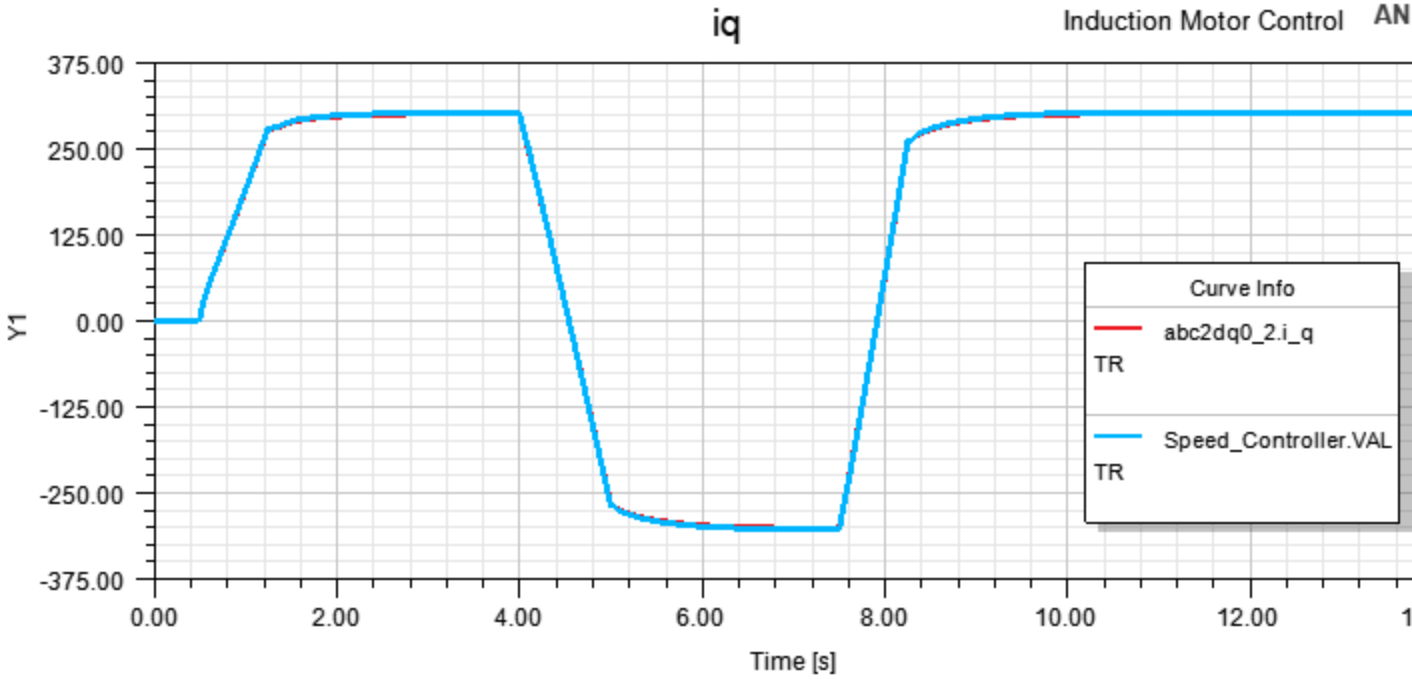
Ramp up at t = 7.5s, from -5 to 5 rad/s, within 0.75 sec

Simulation Results

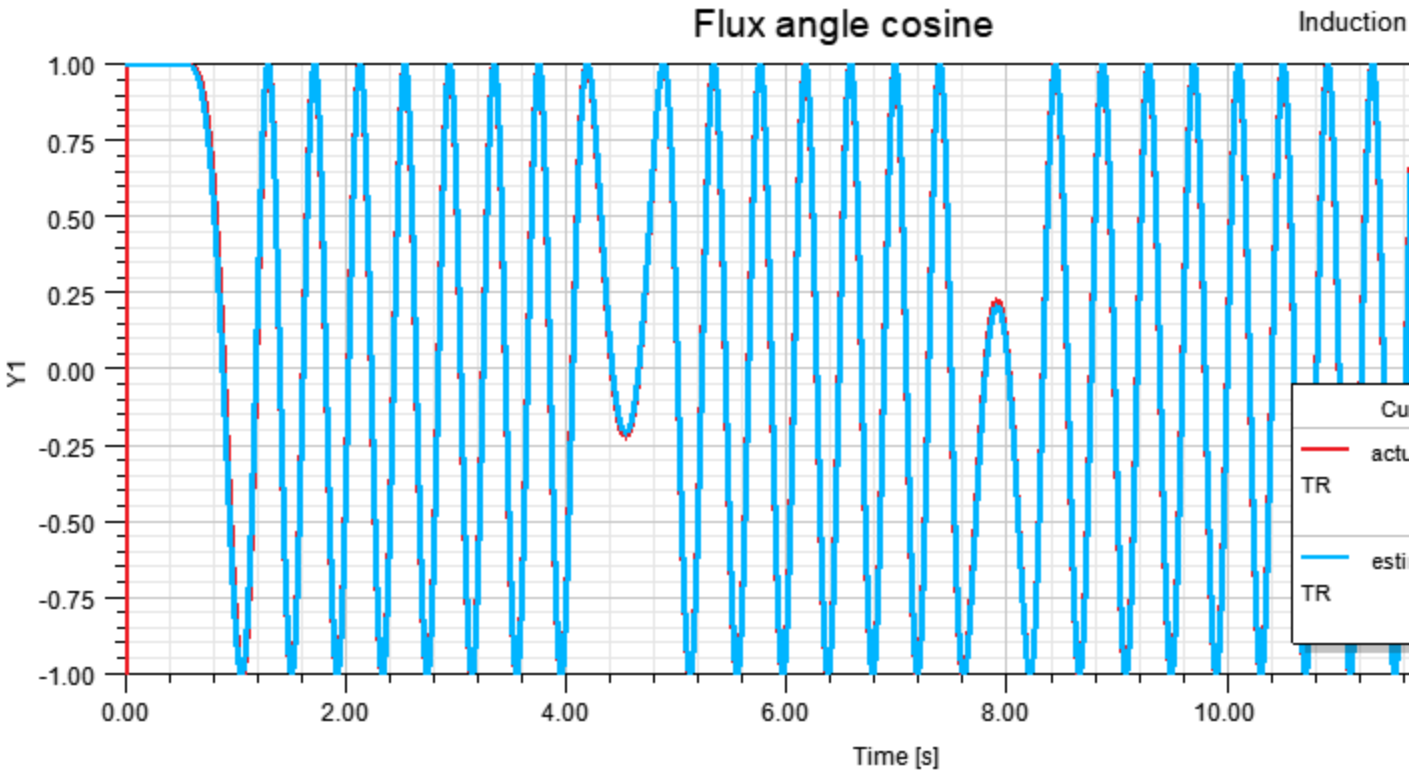
The reference and actual speeds of the induction motor are shown in the following figure:

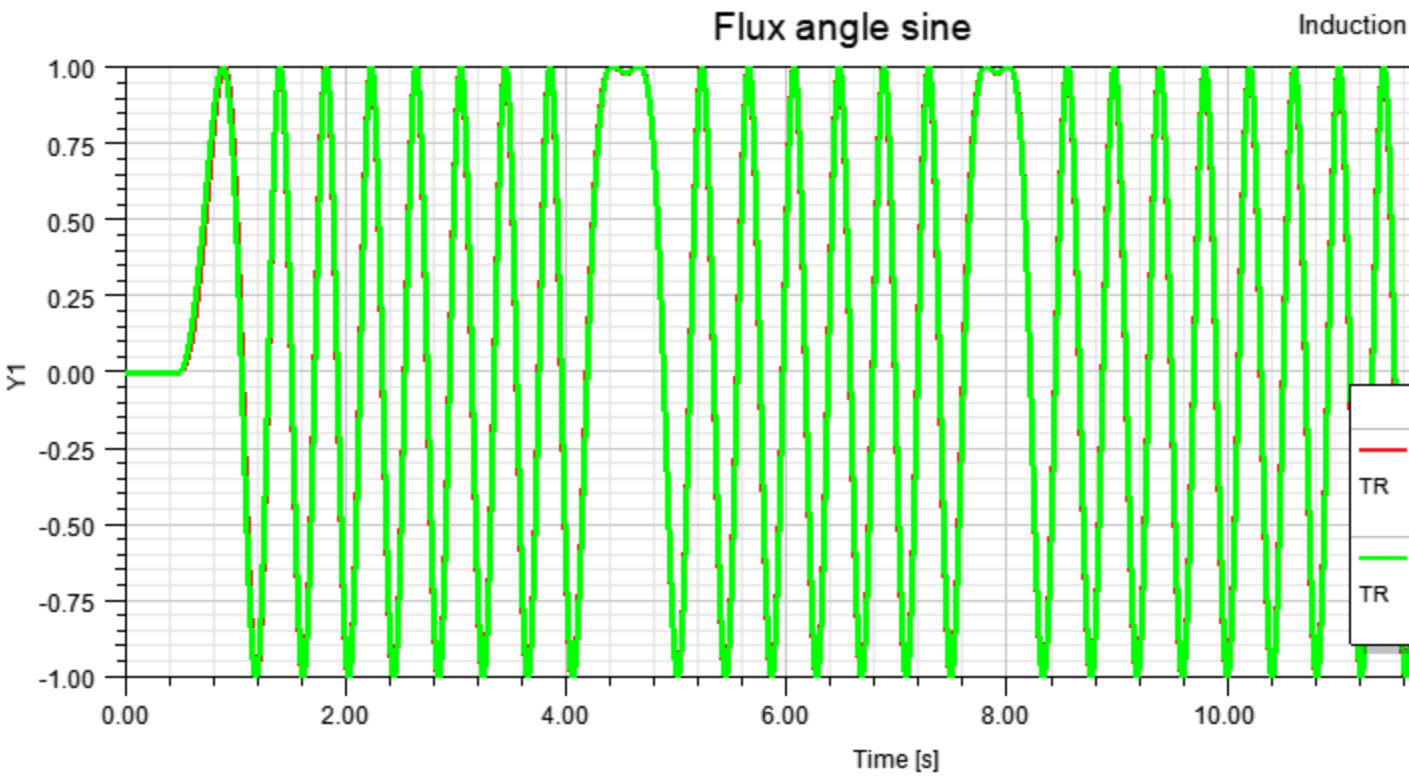






The comparison between the actual and observed flux angle can also be seen in the following figures, which show the sine and cosine of both angles:





Reference:

[1] Yousef, Ayman & Abdel maksoud, Samir. (2015). *Review on Field Oriented Control of Induction Motor*. International Journal for Research in Emerging Science and Technology (IJREST). 2.

[2] Vas, P. *Electrical Machines and Drives: A Space-vector Theory Approach.* New York: Oxford University Press, 1992.

Mutual Inductor Example

Description

The Mutual Inductor schematic is shown in Figure 1.

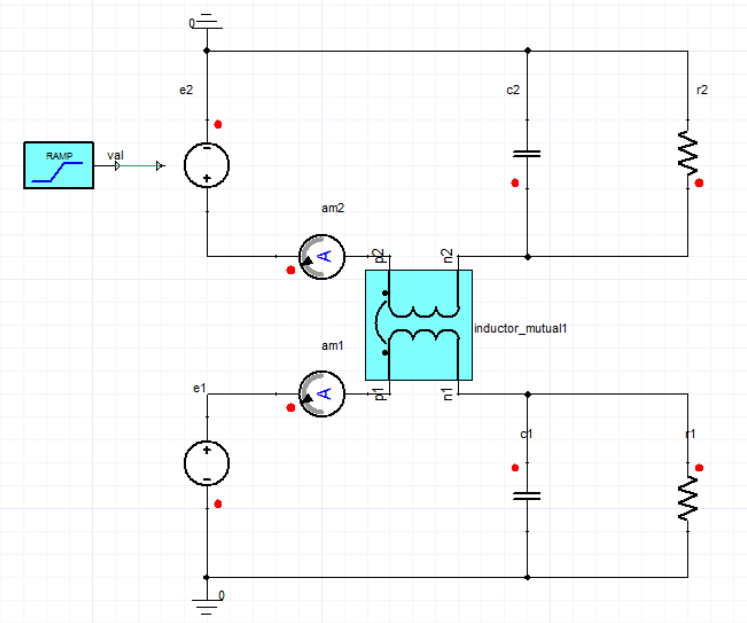


Figure 1: Mutual InductorSchematic

The system contains theinductor_mutualmodel from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofmutual inductor component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The currents comparison is shown in Figure 2.

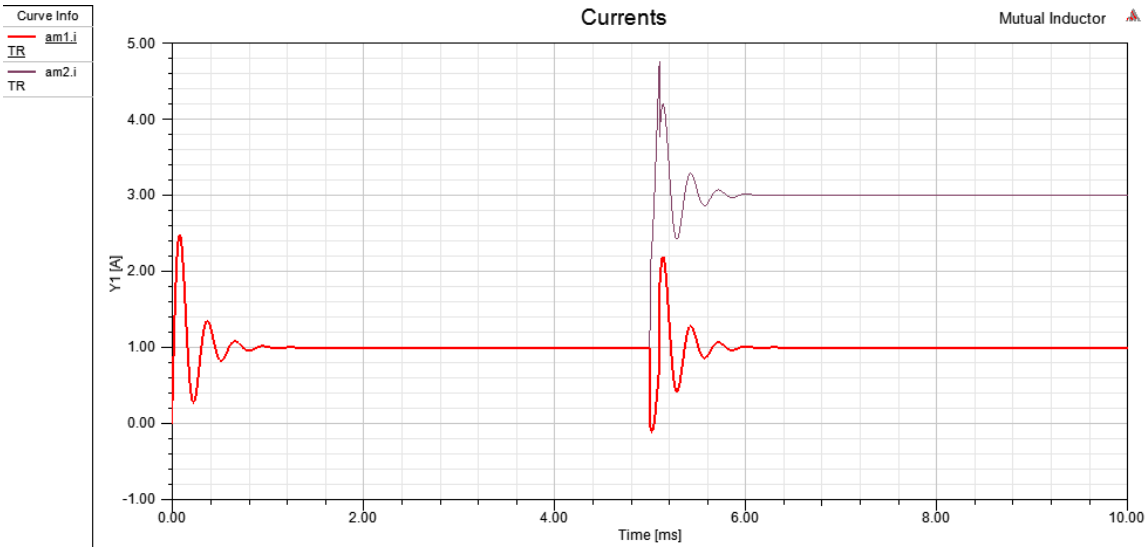


Figure 2: Current Comparison

Full Bridge Resonant Converter Example

Description

The full bridge resonant converter schematic is shown in Figure 1.

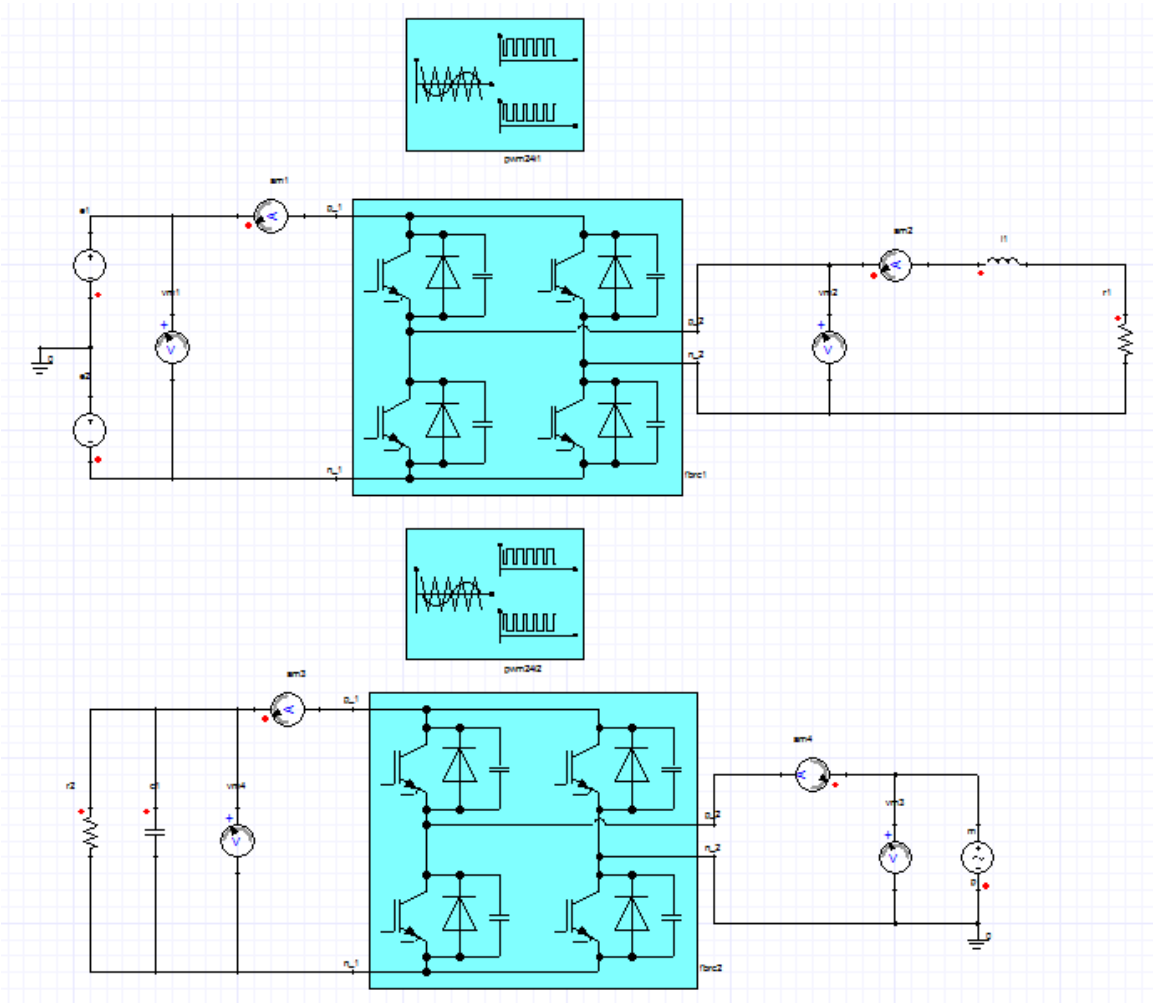


Figure 1: Full Bridge Resonant Converter Schematic

The system contains the pwm24i and fbrcmodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 2 level full bridge resonant converter and the 2 level 4 pulse PWM generator in the Power System VHDL-AMS library.

fbrc can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the fbrc component as an inverter and the lower circuit shows the usage of the fbrc component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

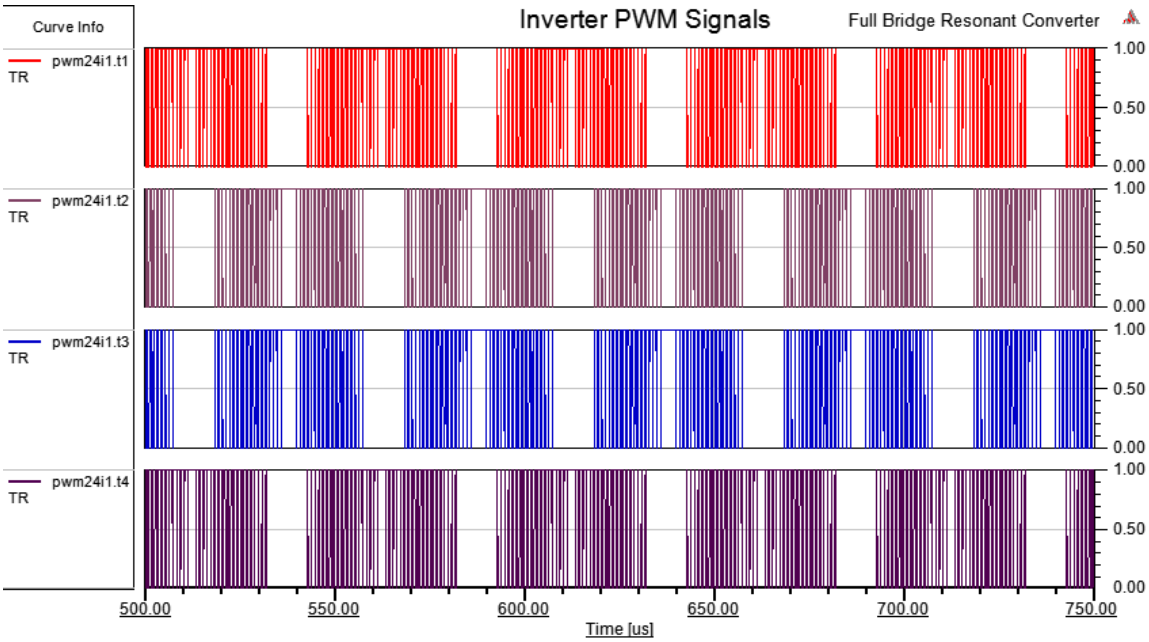


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

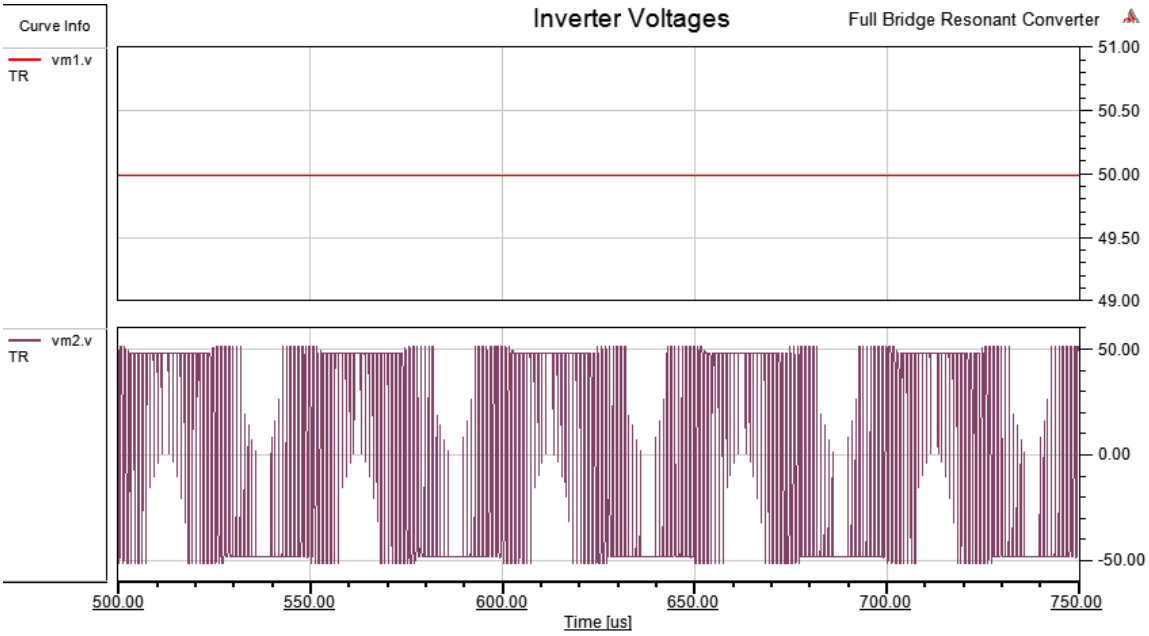


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

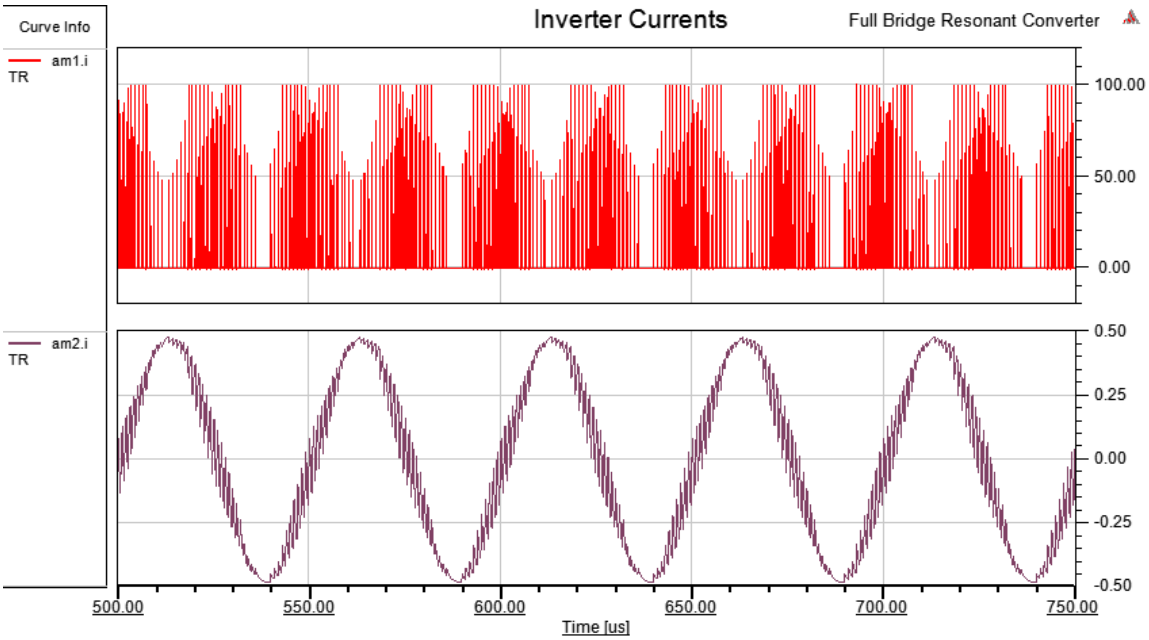


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

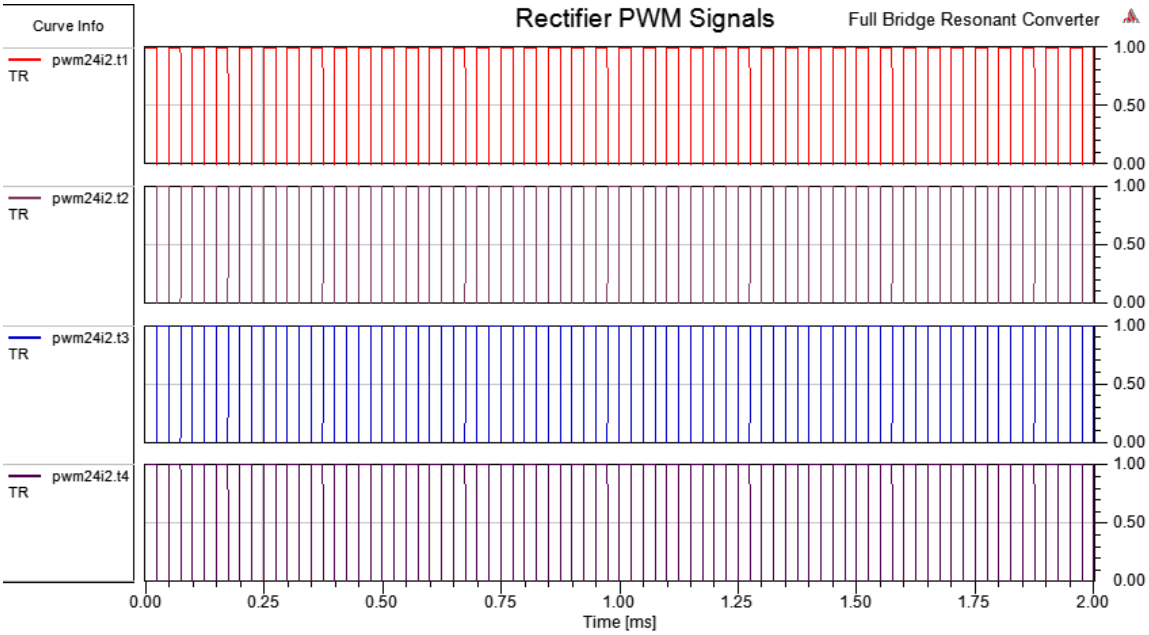


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

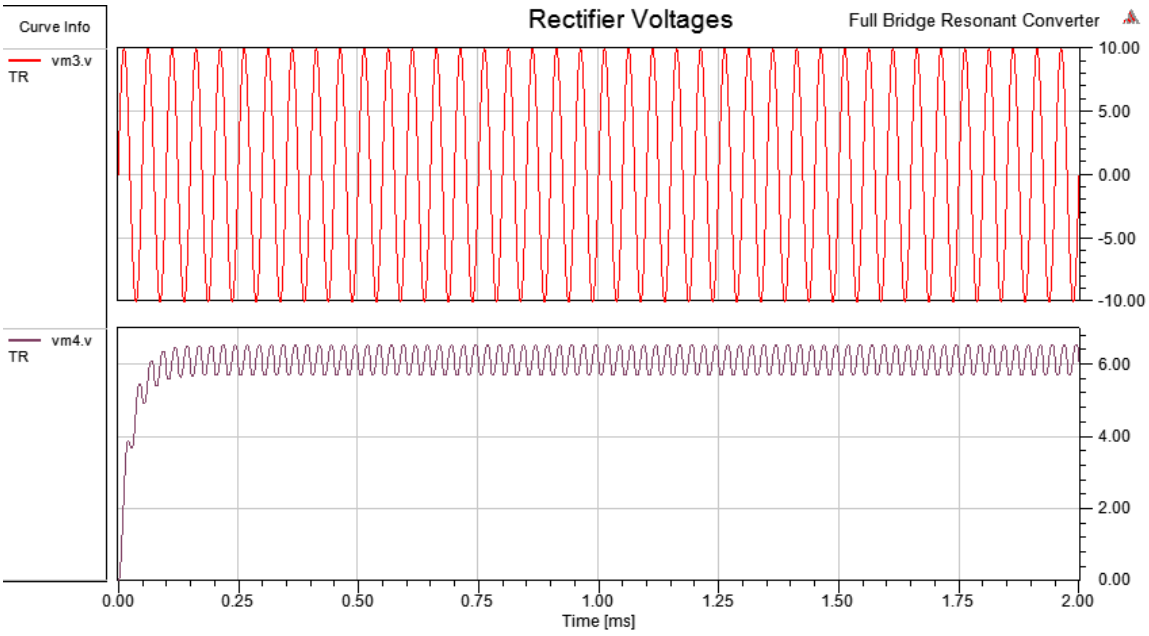


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

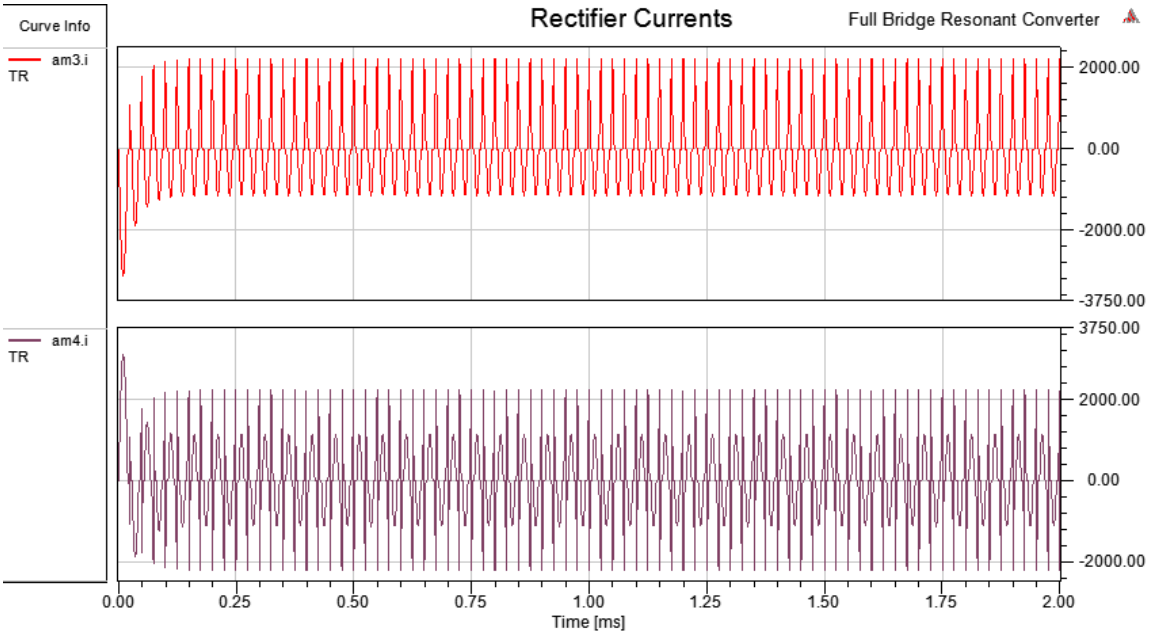


Figure 7: Rectifier Input/Output Currents

Load Full Bridge Resonant Converter Example

Half Bridge Resonant Converter Example

Description

The half bridge resonant converter schematic is shown in Figure 1.

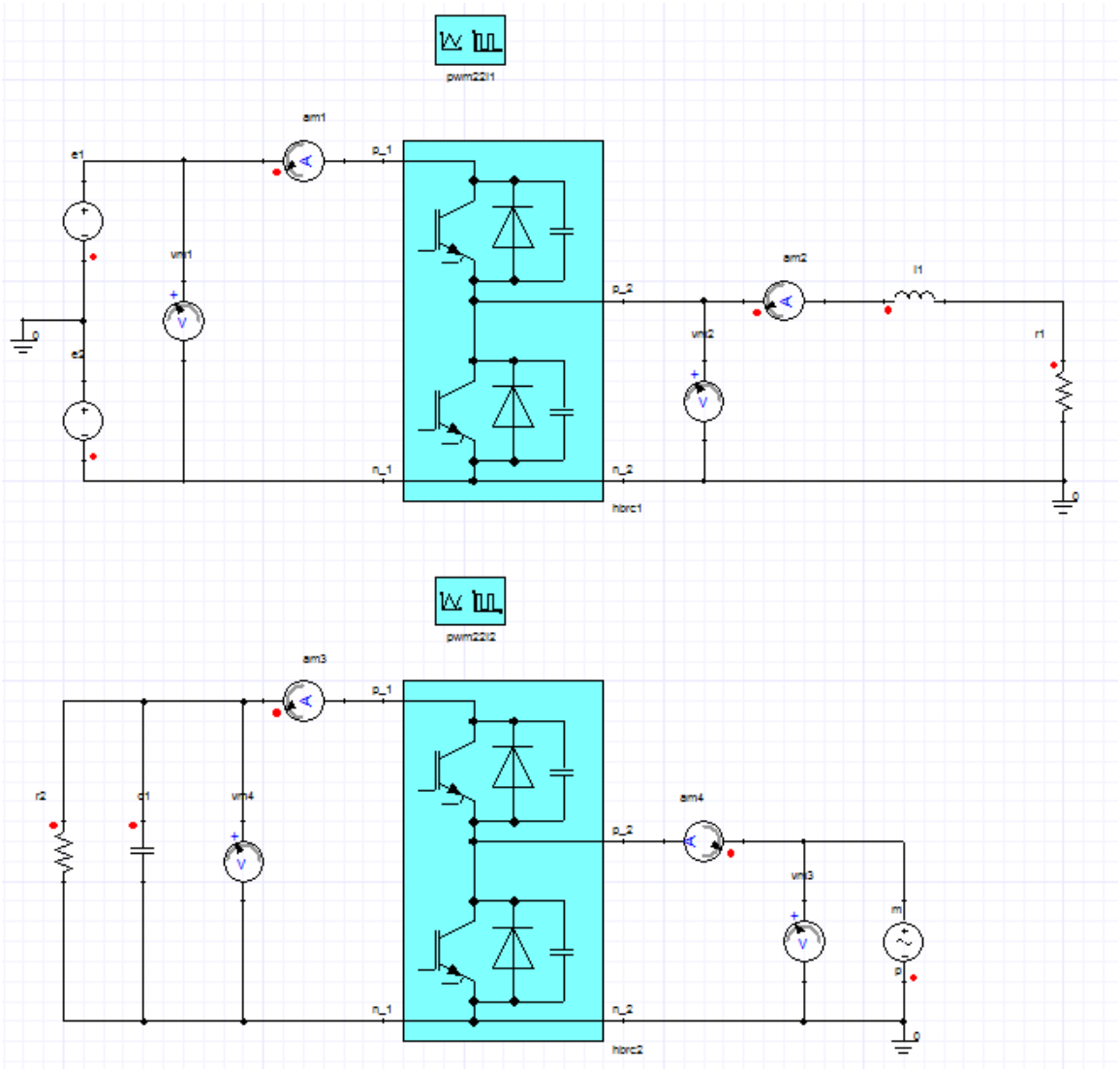


Figure 1: Half Bridge Resonant Converter Schematic

The system contains the pwm22i and hbrcmodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 2 level half bridge resonant converter and the 2 level 2 pulse PWM generator in the Power System VHDL-AMS library.

hbrc can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the hbrc component as an inverter and the lower circuit shows the usage of the hbrc component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

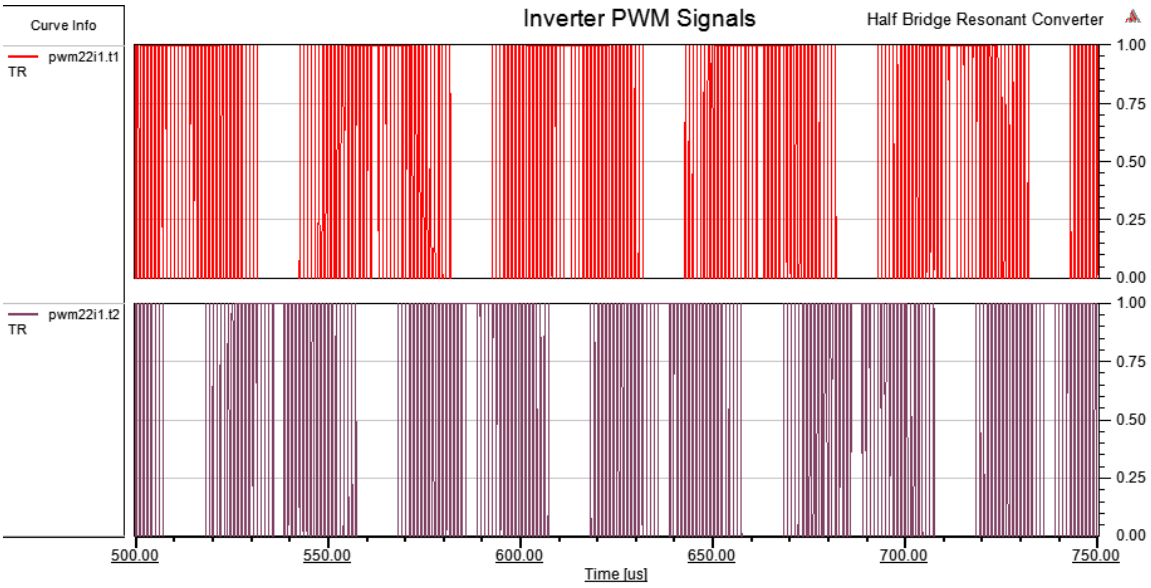


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

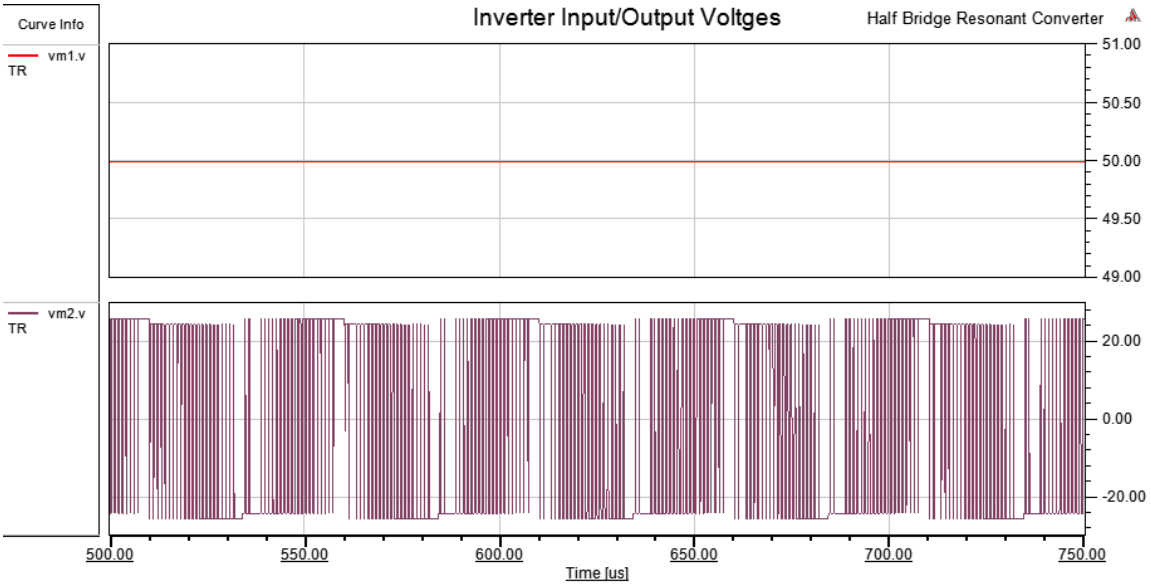


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

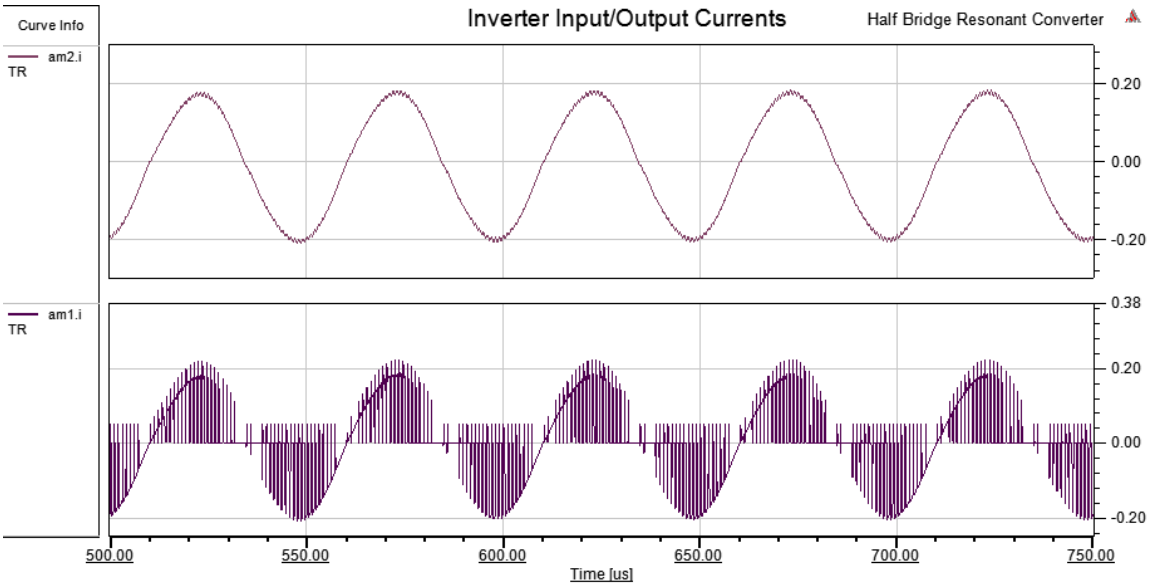


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

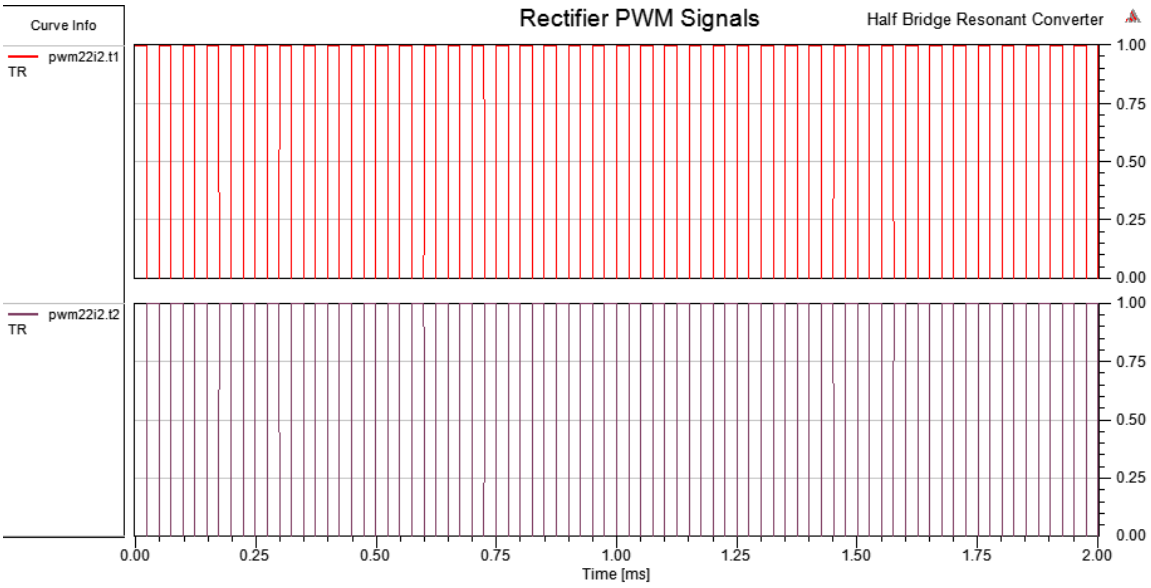


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

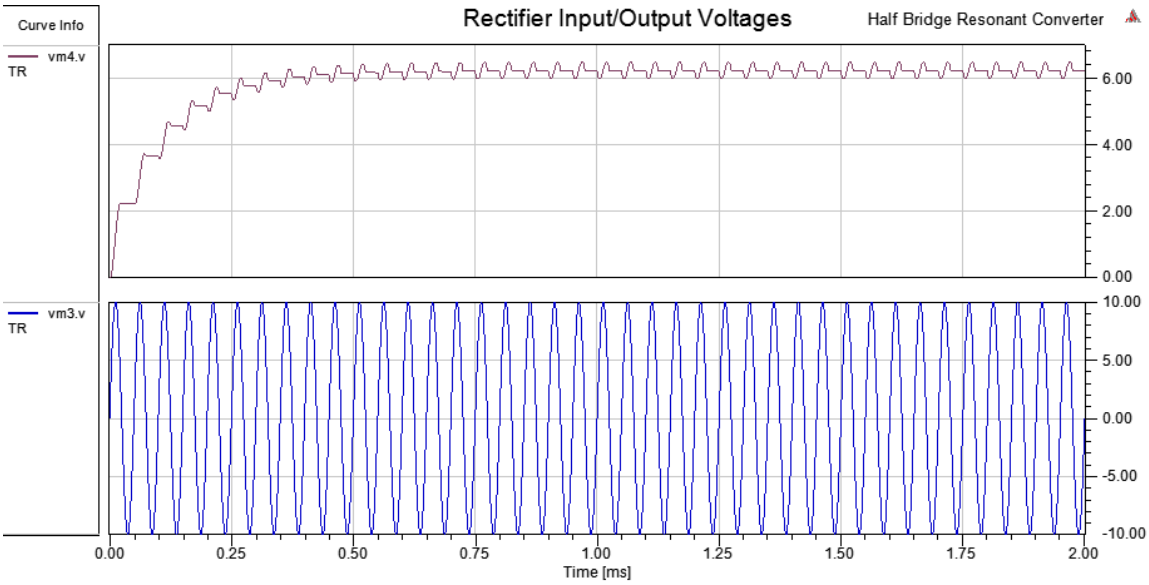


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

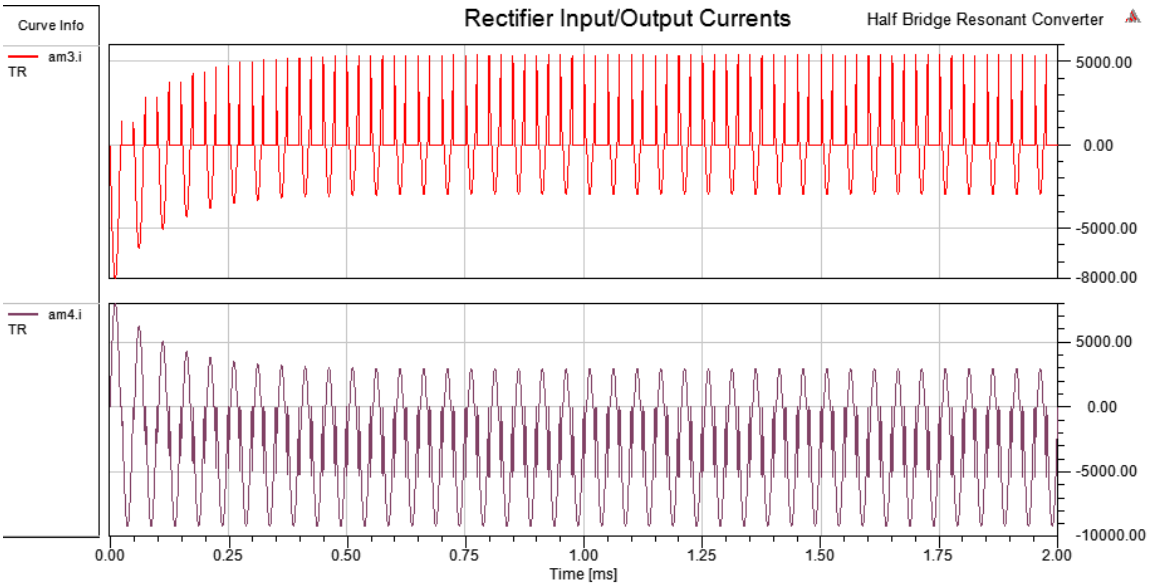


Figure 7: Rectifier Input/Output Currents

Load Half Bridge Resonant Converter Example

Rotational Electromechanical Converter Example

Description

The Rotational Electromechanical Converter schematic is shown in Figure 1.

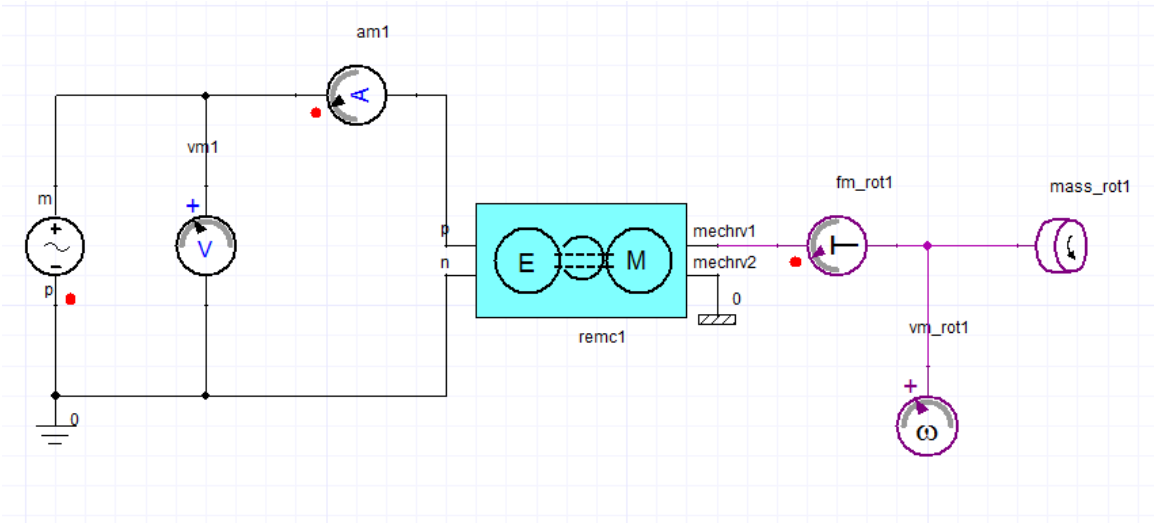


Figure 1: Rotational Electromechanical ConverterSchematic

The system contains theremcmodel from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofrotational electromechanical converter component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The electrical measurements are shown in Figure 2.

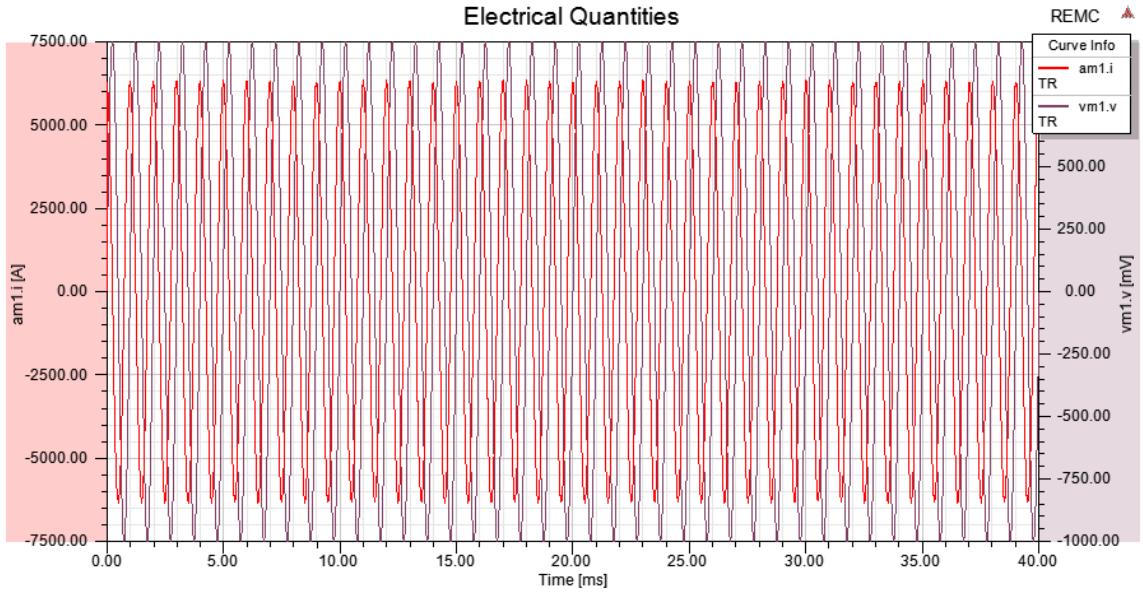


Figure 2: Electrical Measurements

The mechanical measurements are shown in Figure 3.

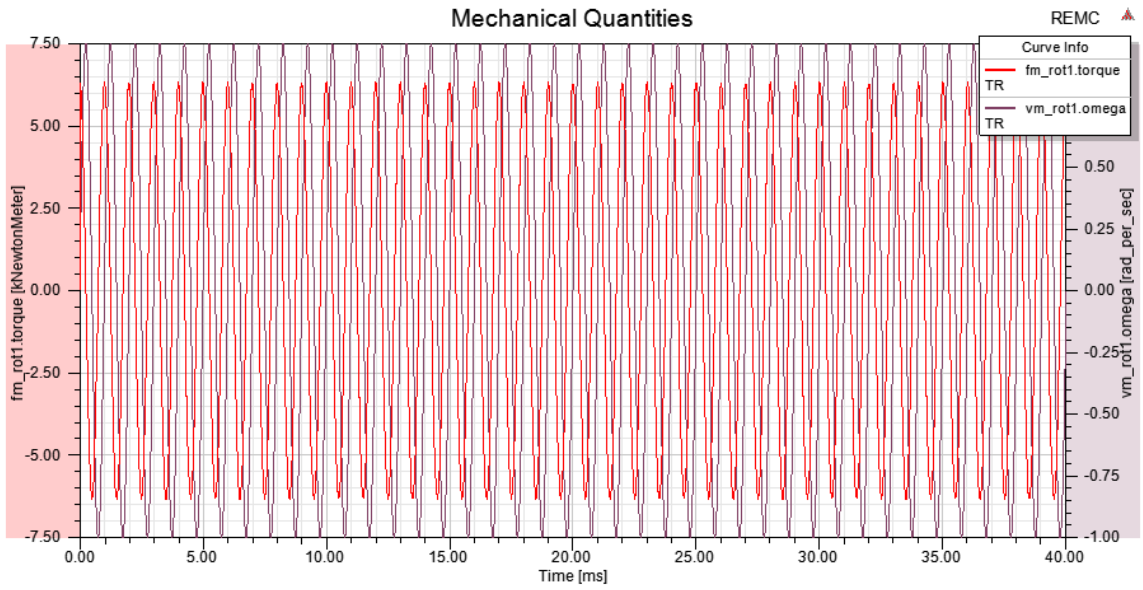


Figure 3: Mechanical Measurements

The power comparison isshown in Figure 4.

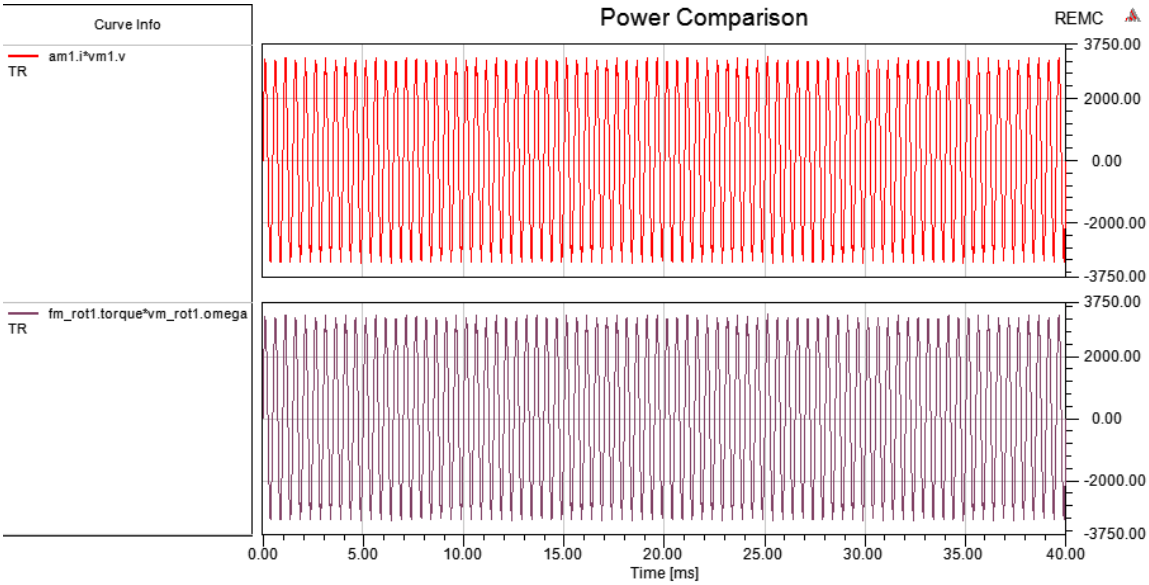


Figure 4: Power Comparison

Simple ElectroMagnetic Example

Description

The Simple ElectroMagnetic schematic is shown in Figure 1.

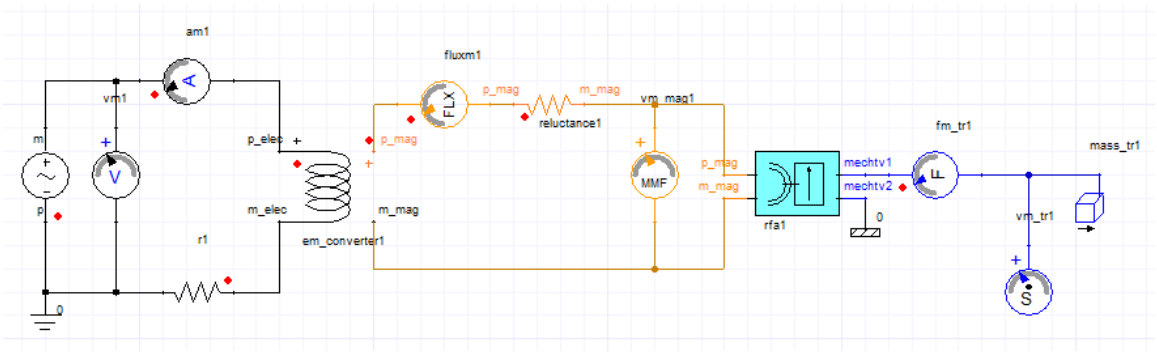


Figure 1: Simple ElectroMagneticSchematic

The system contains theem_converter and rfa models from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofelectromagnetic related basic components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The electrical measurements are shown in Figure 2.

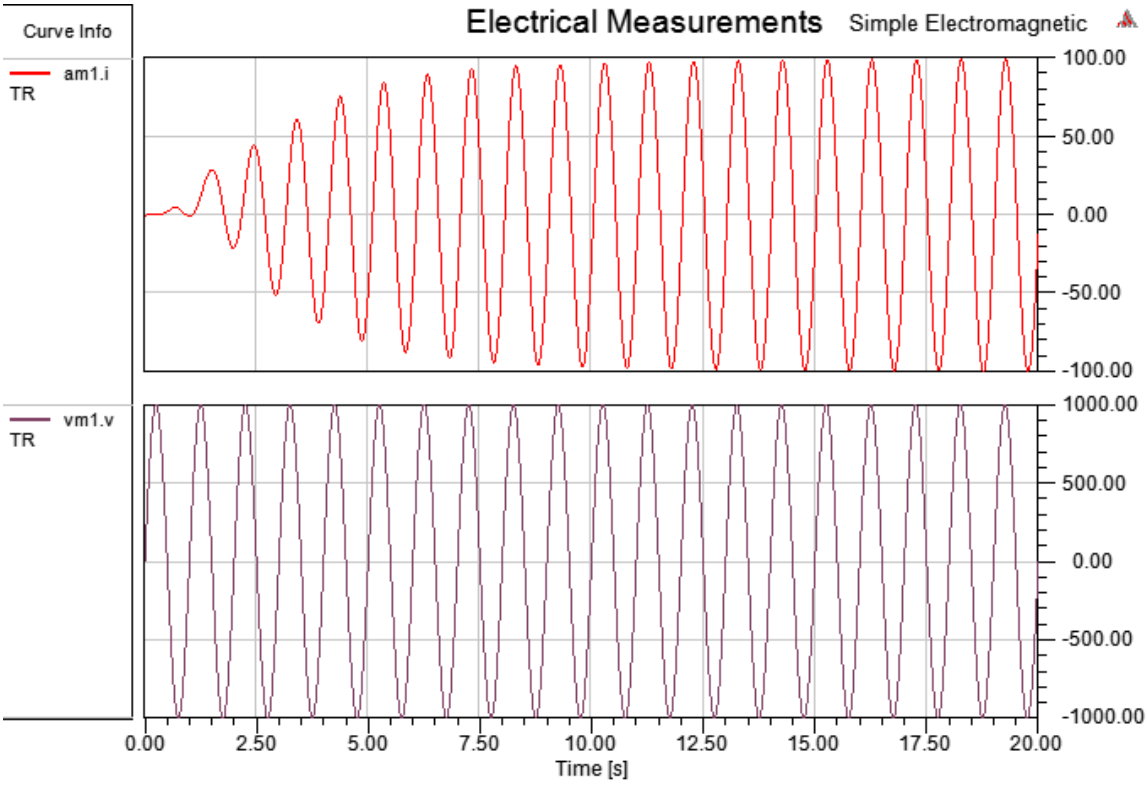


Figure 2: Electrical Measurements

The magnetic measurements are shown in Figure 3.

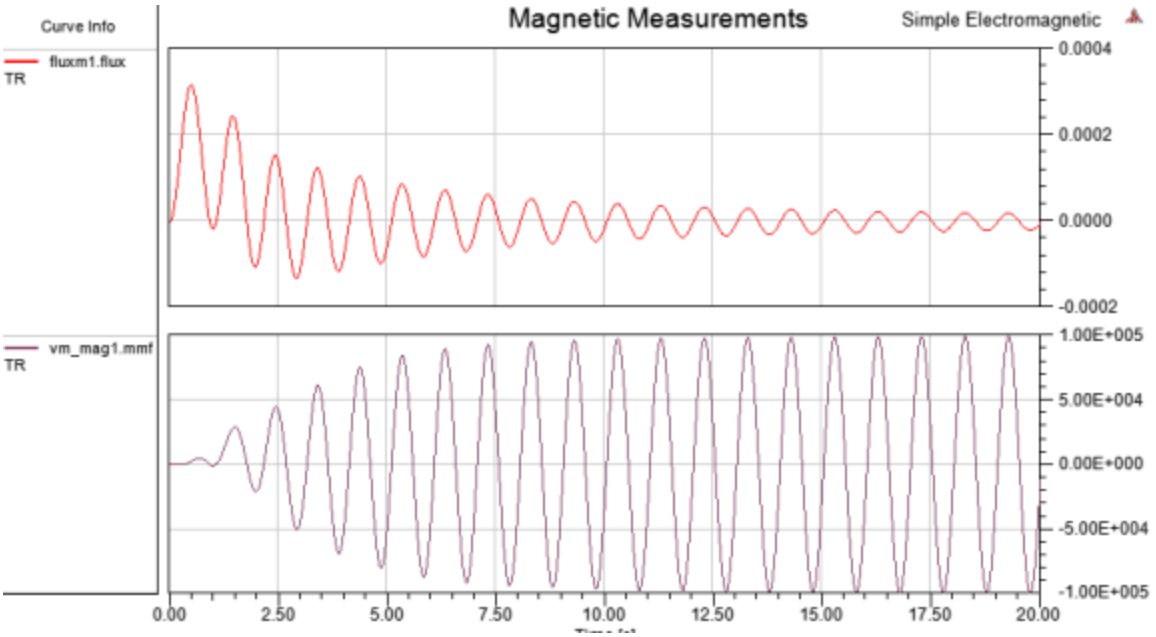


Figure 3: Magnetic Measurements

The mechanical measurements are shown in Figure 4.

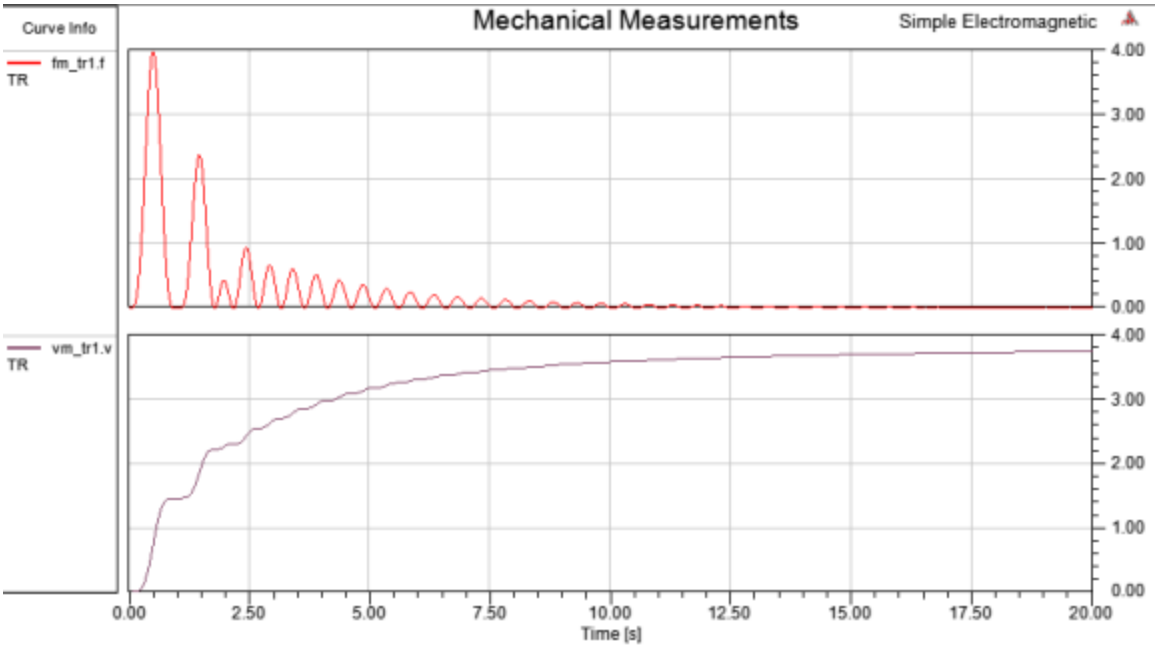


Figure 4: Mechanical Measurements

Simple Transformer Example

Description

The simple transformer schematic is shown in Figure 1.

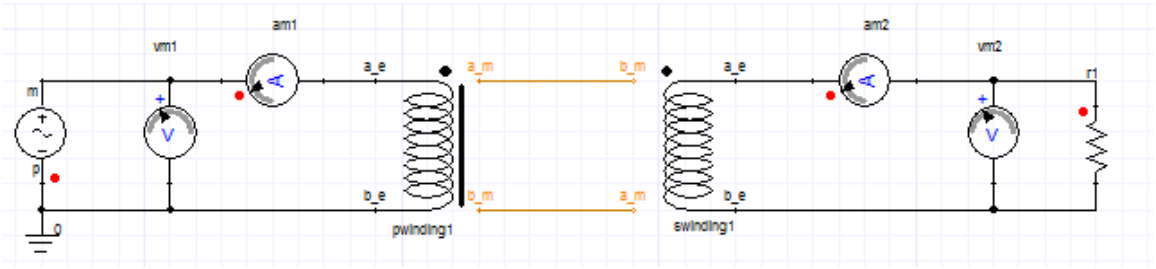


Figure 1: Simple Transformer Schematic

The system contains the pwinding and swindingmodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of primary and secondary winding components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The current comparison results are shown in Figure 2.

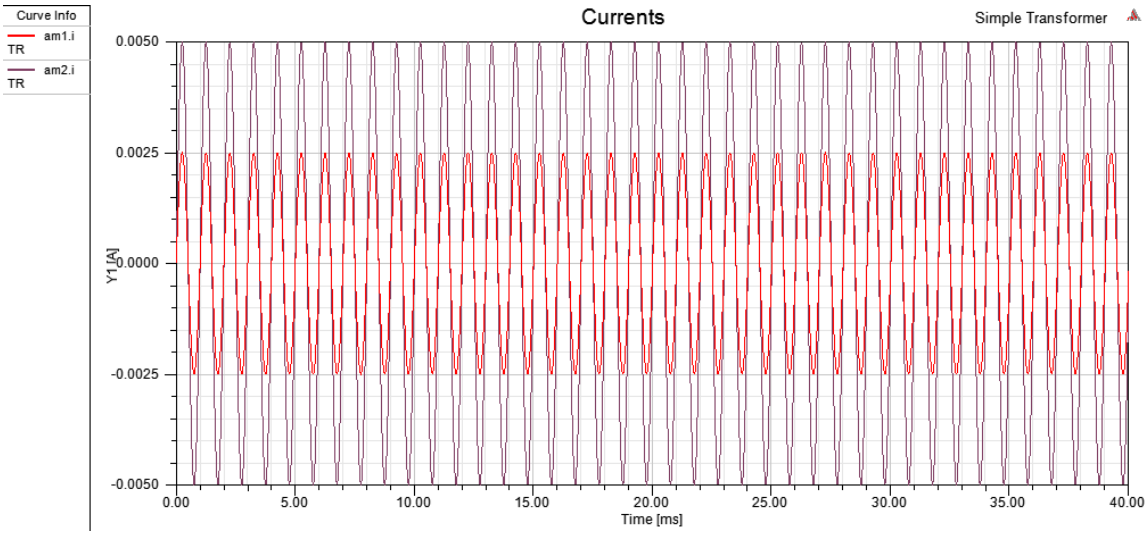


Figure 2: Current Comparison

The voltage comparison results are shown in Figure 3.

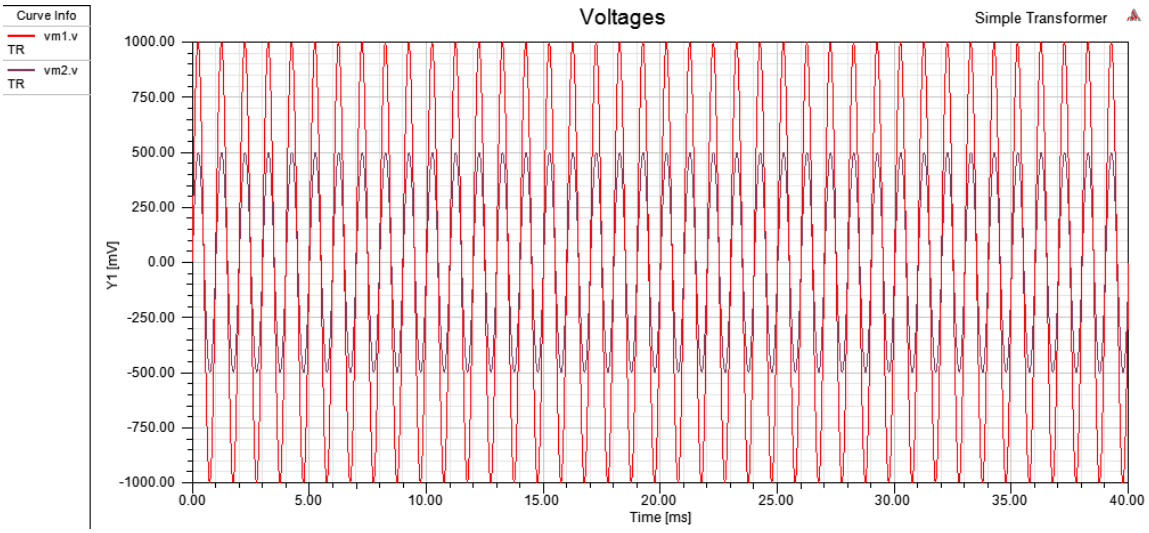


Figure 3: Voltage Comparison

Space Vector PWM Example

Description

The Space Vector PWM schematic is shown in Figure 1.

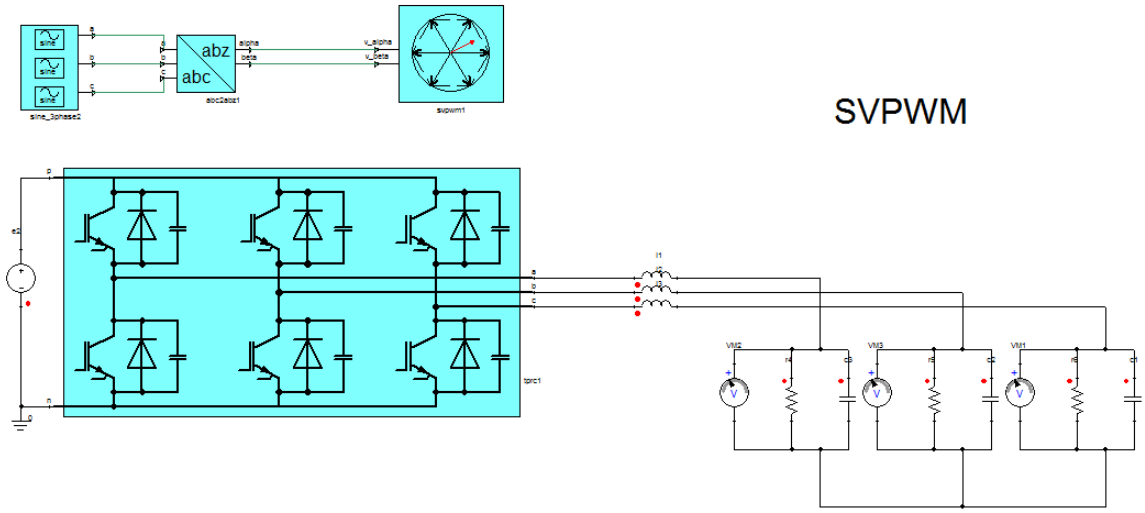


Figure 1: Space Vector PWM Schematic

The system contains the sine_3phase, abc2abz, svpwm and tprc models from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of space vector PWM component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The Input signals and load voltages are shown in Figure 2.

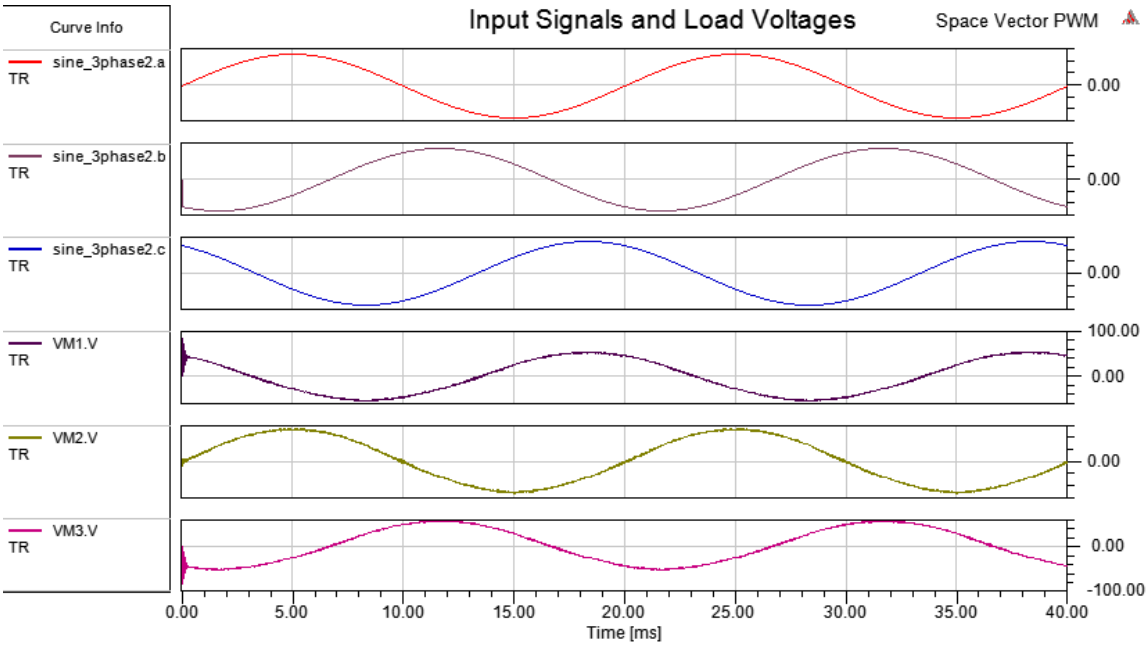


Figure 2: Input Signals and Load Voltages

The Alpha-Beta-Zero references to the svpwm component are shown in Figure 3.

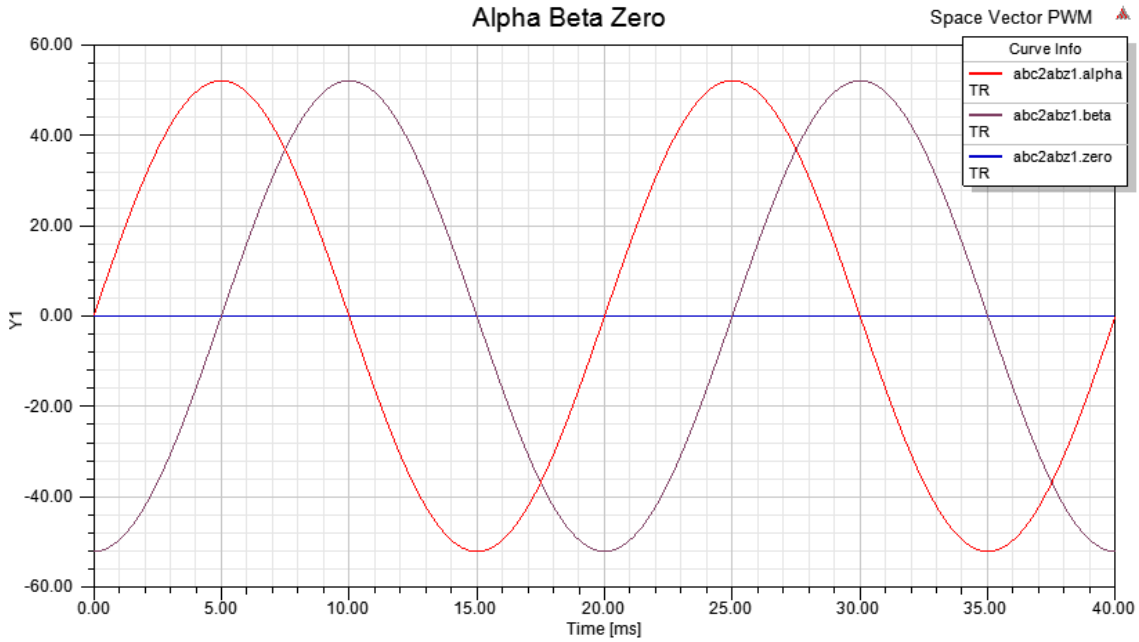


Figure 3: Alpha-Beta-Zero Signals

The SVPWM control signals are shown in Figure 4.

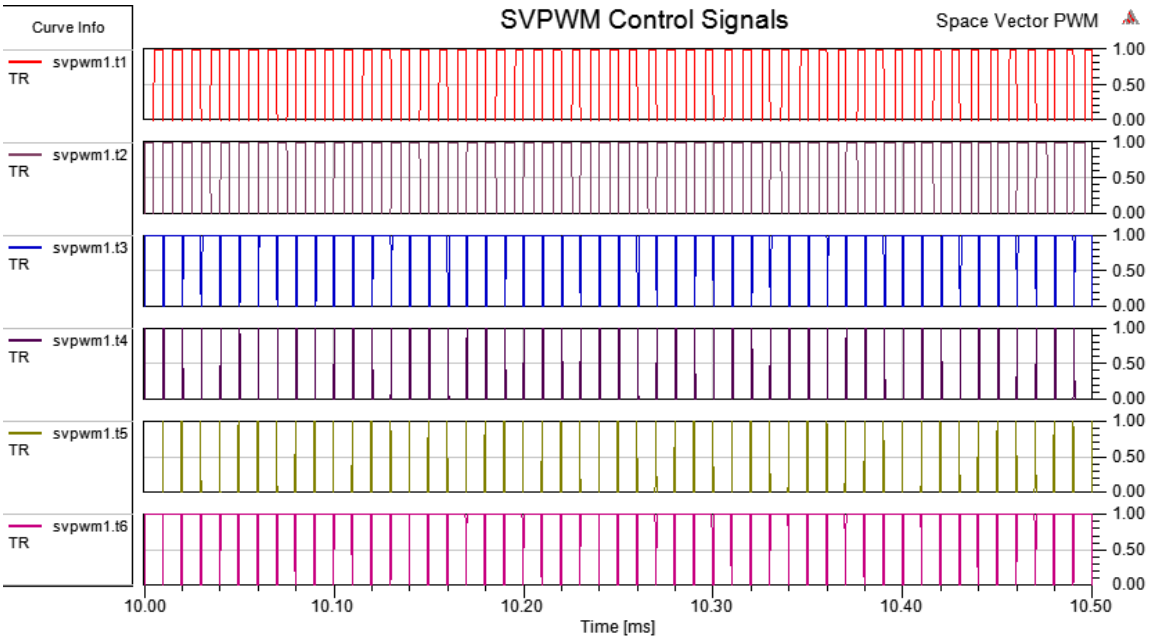


Figure 4: SVPWM Control Signals

Switches Example

Description

The switches schematic is shown in Figure 1.

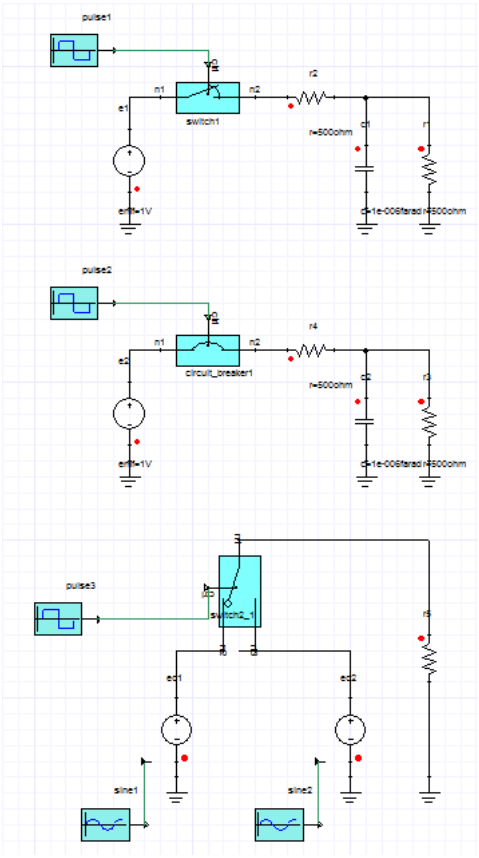


Figure 1: SwitchesSchematic

The system contains theswitch, circuit_breaker and switch2 models from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage of switches in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The control signal vs. load voltages comparison of Switch circuit is shown in Figure 2.

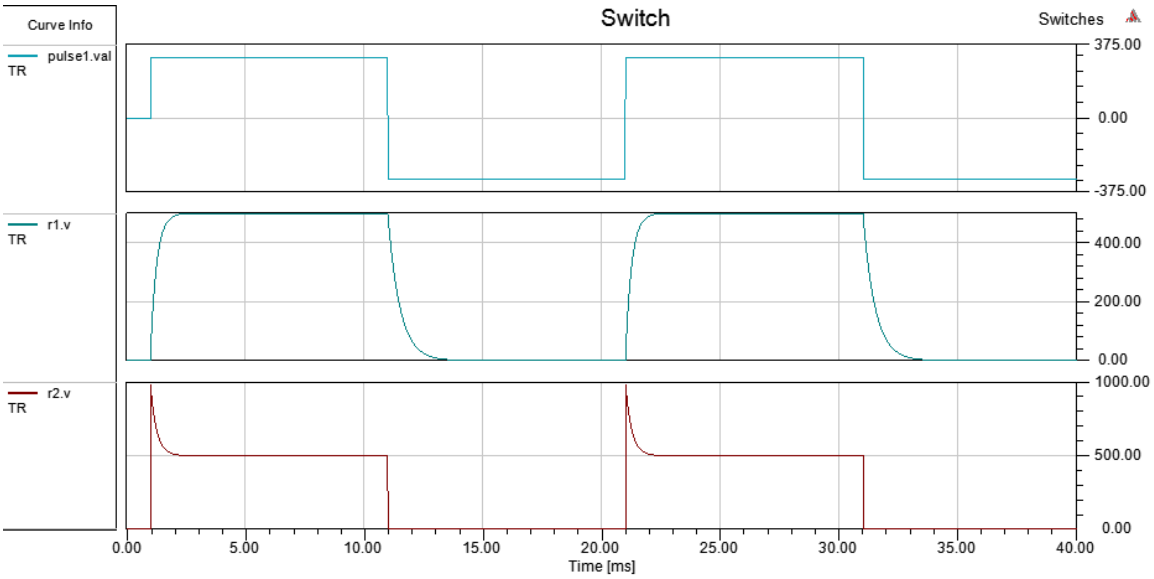


Figure 2: Switch

The control signal vs. load voltages comparison of Circuit Breaker circuit is shown in Figure 3.

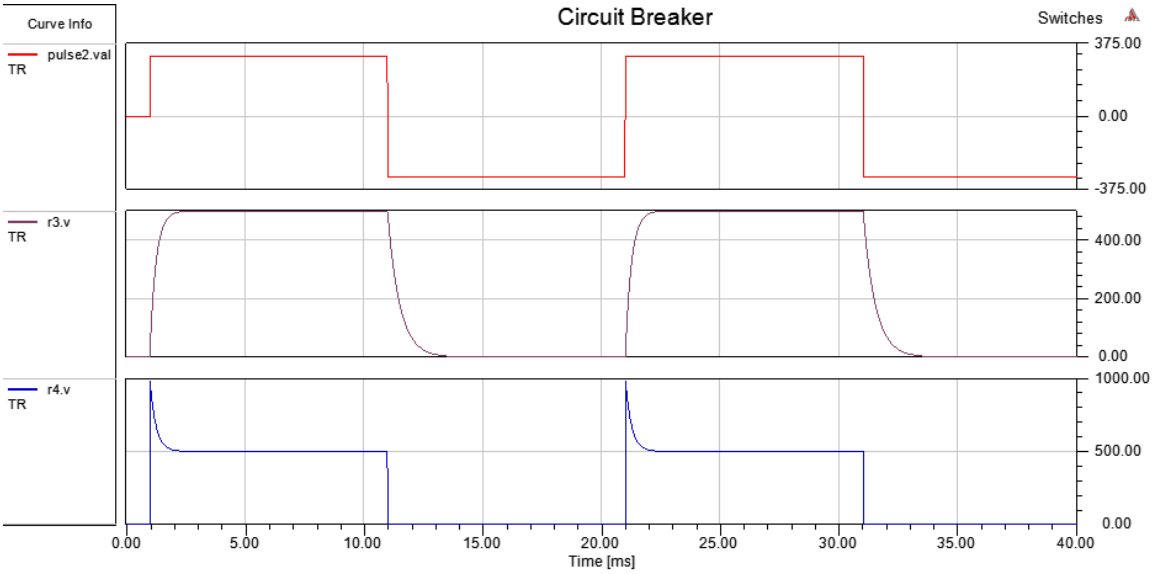


Figure 3: Circuit Breaker

The control signal vs. load voltages comparison of Two Way Switch circuit is shown in Figure 4.

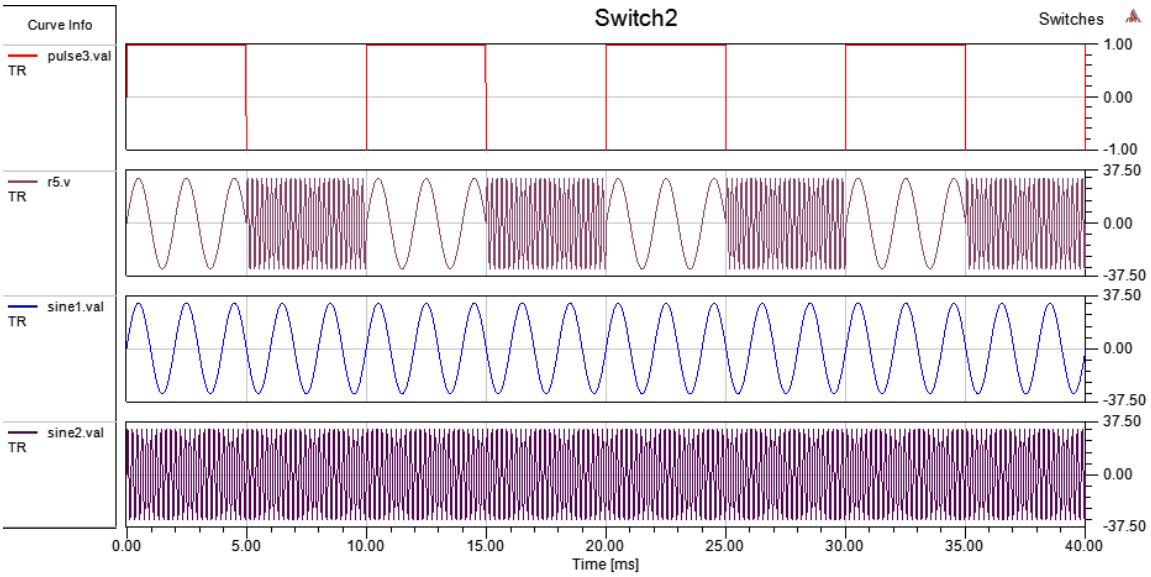


Figure 4: Two Way Switch

Three Level Eight Pulse PWM Example

Description

The threelevel eight pulse PWM schematic is shown in Figure 1.

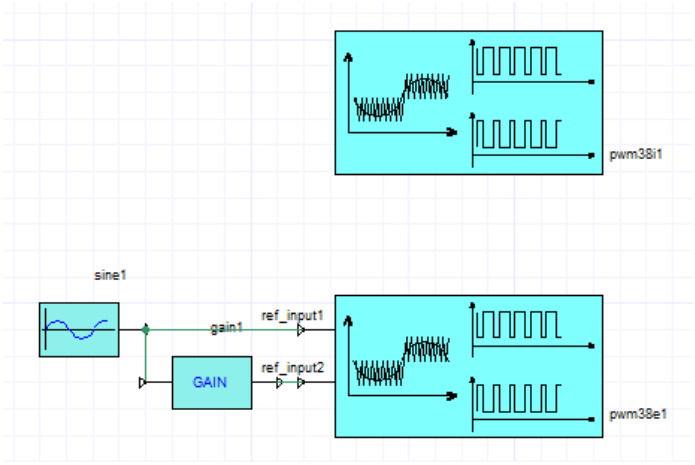


Figure 1: Three Level Eight Pulse PWM Schematic

The system contains the pwm38i and pwm38emodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of three level eight pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The control signalsgenerated by pwm38i are shown in Figure 2.

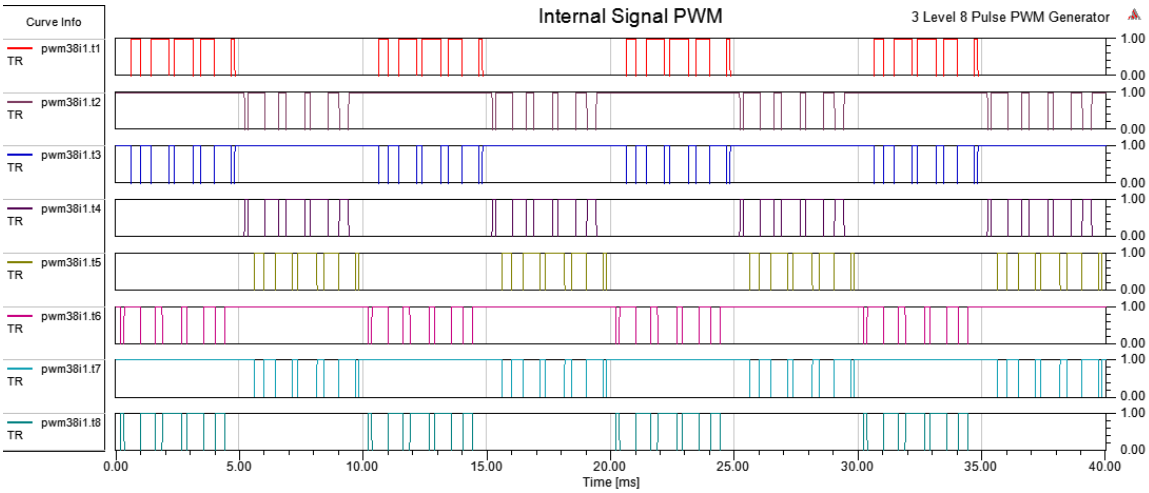


Figure 2: Internal Signal PWM

The control signals generated by pwm38e are shown in Figure 3.

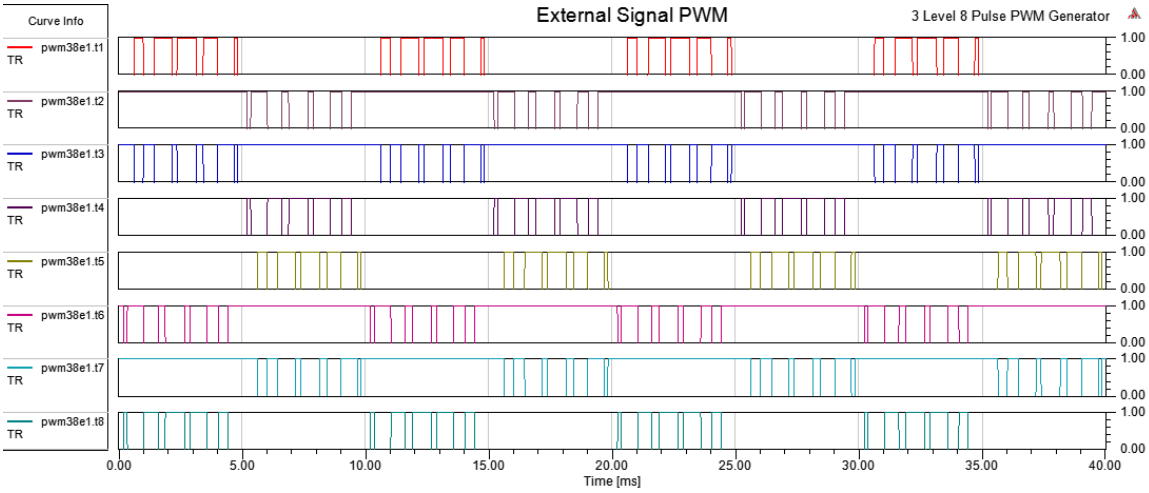


Figure 3: External Signal PWM

Three Level Four Pulse PWM Example

Description

The threelevel four pulse PWM schematic is shown in Figure 1.

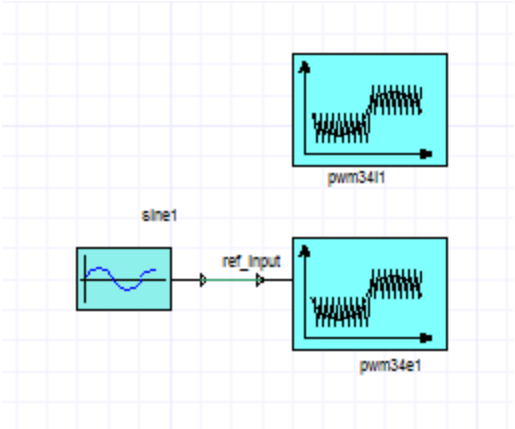


Figure 1: Three Level Four Pulse PWM Schematic

The system contains the pwm34i and pwm34emodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of three level four pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The control signals generated by pwm34i are shown in Figure 2.

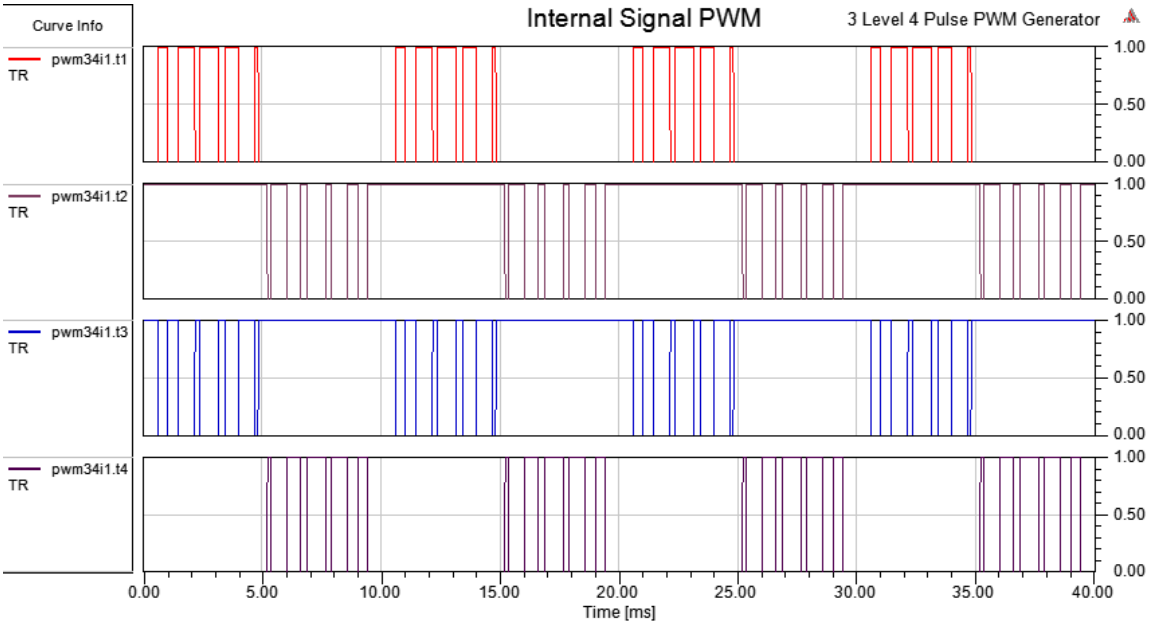


Figure 2: Internal Signal PWM

The control signals generated by pwm34e are shown in Figure 3.

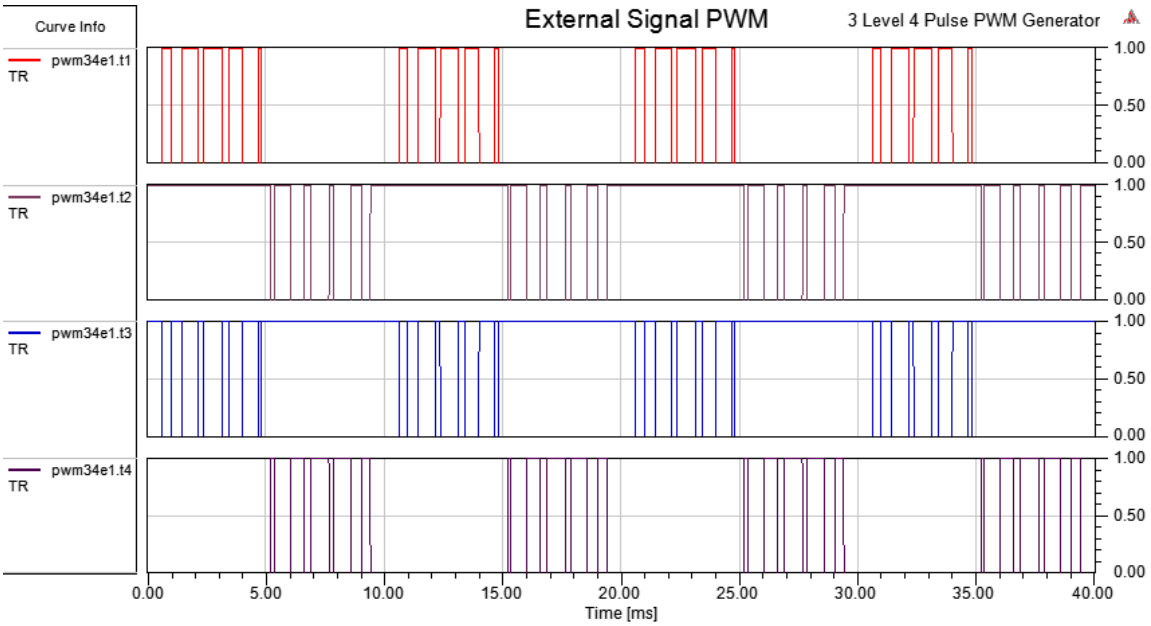


Figure 3: External Signal PWM

Three Level Full Bridge Resonant Converter Example

Description

The three level full bridge resonant converter schematic is shown in Figure 1.

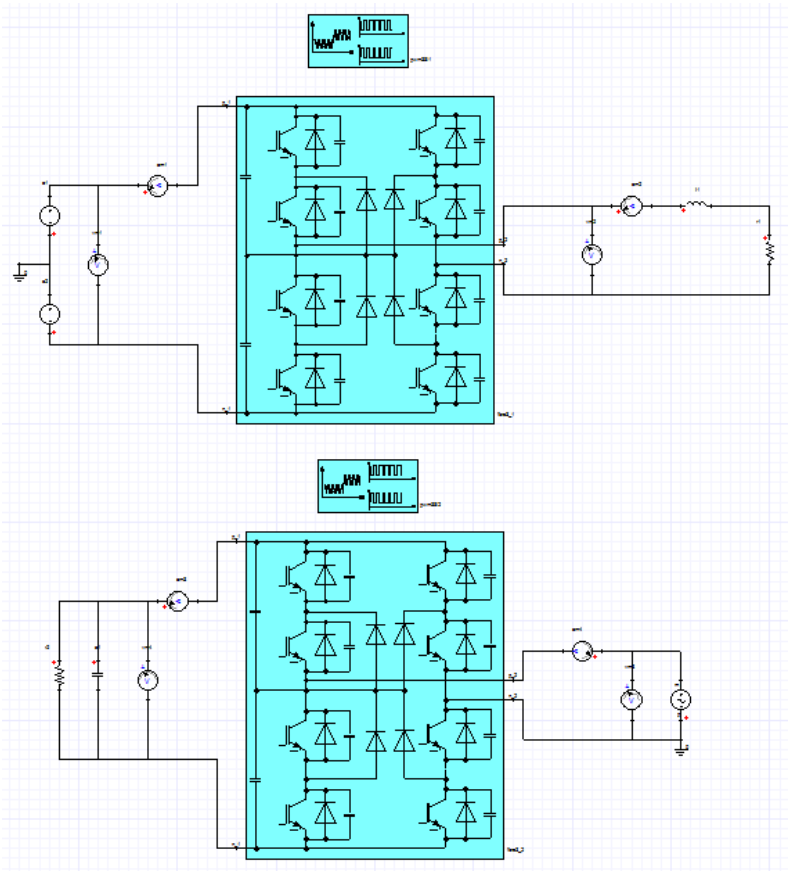


Figure 1: Three Level Full Bridge Resonant Converter Schematic

The system contains the pwm38i and fbrc3models from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 3 level full bridge resonant converter and the 3 level 8 pulse PWM generator in the Power System VHDL-AMS library.

fbrc3 can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the fbrc3 component as an inverter and the lower circuit shows the usage of the fbrc3 component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

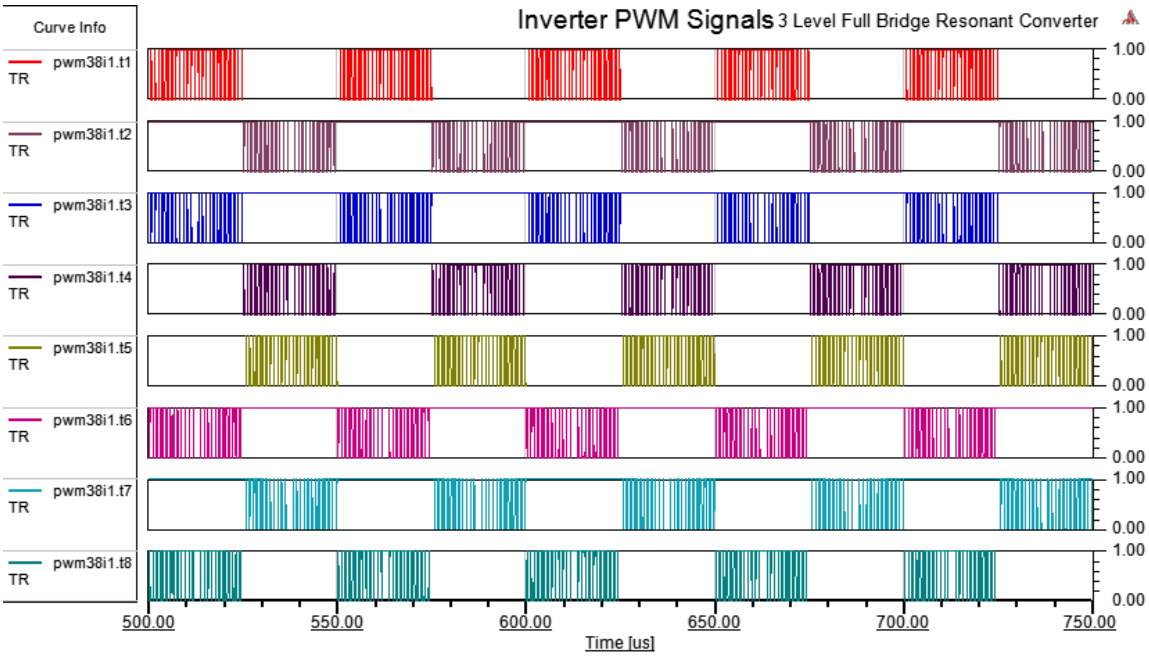


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

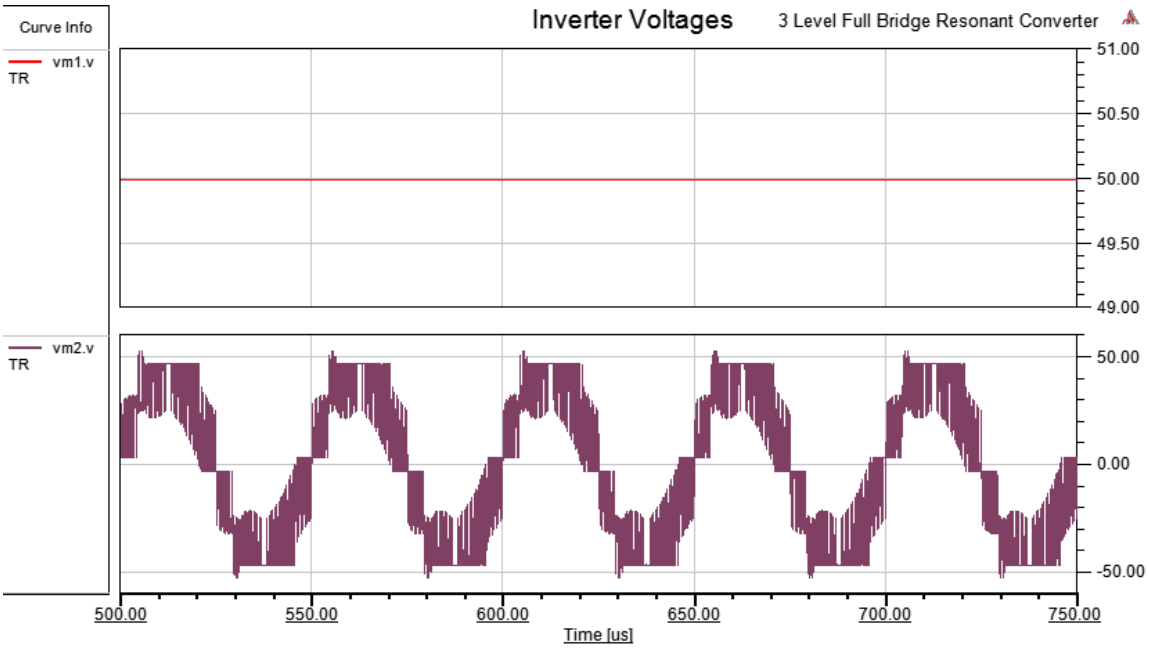


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

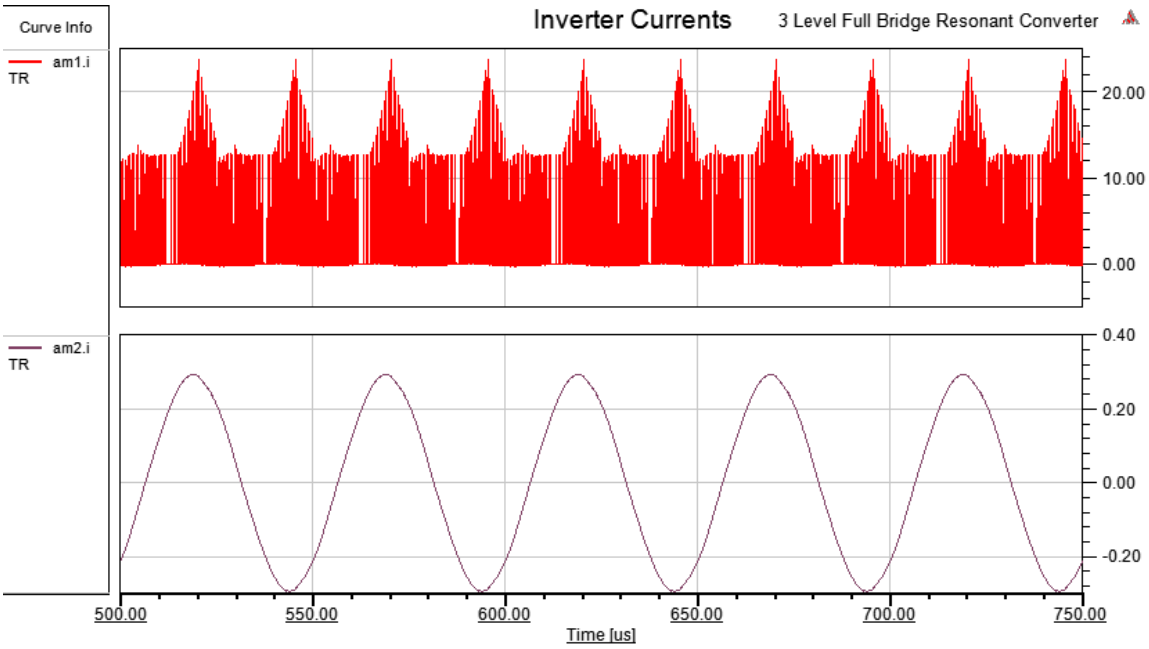


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

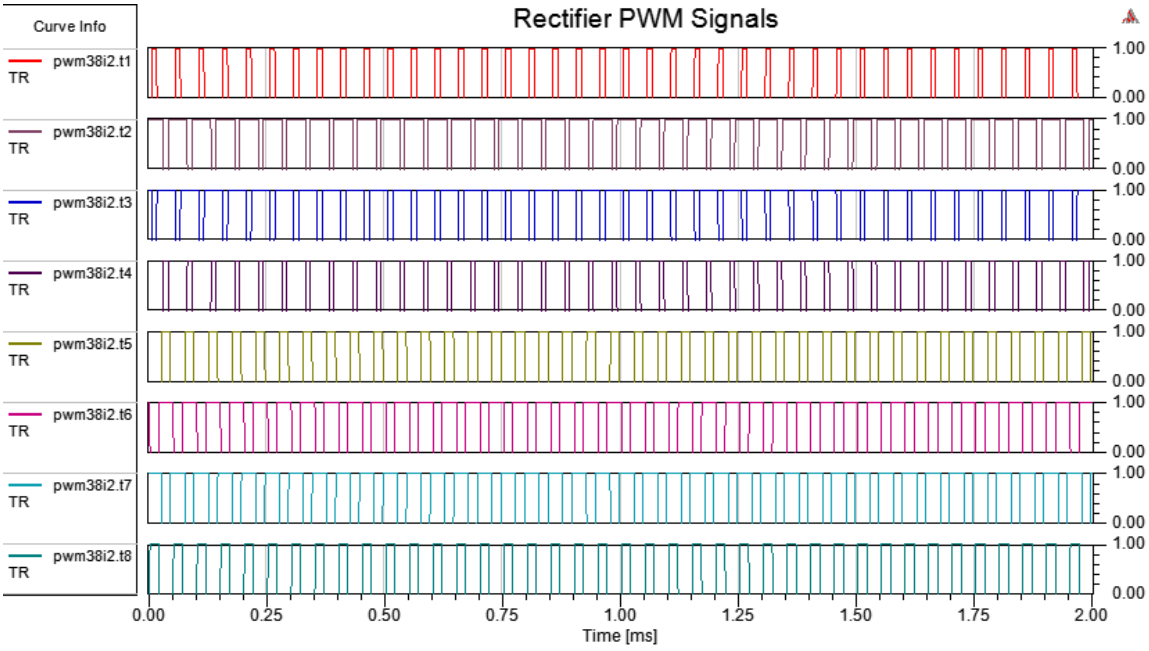


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

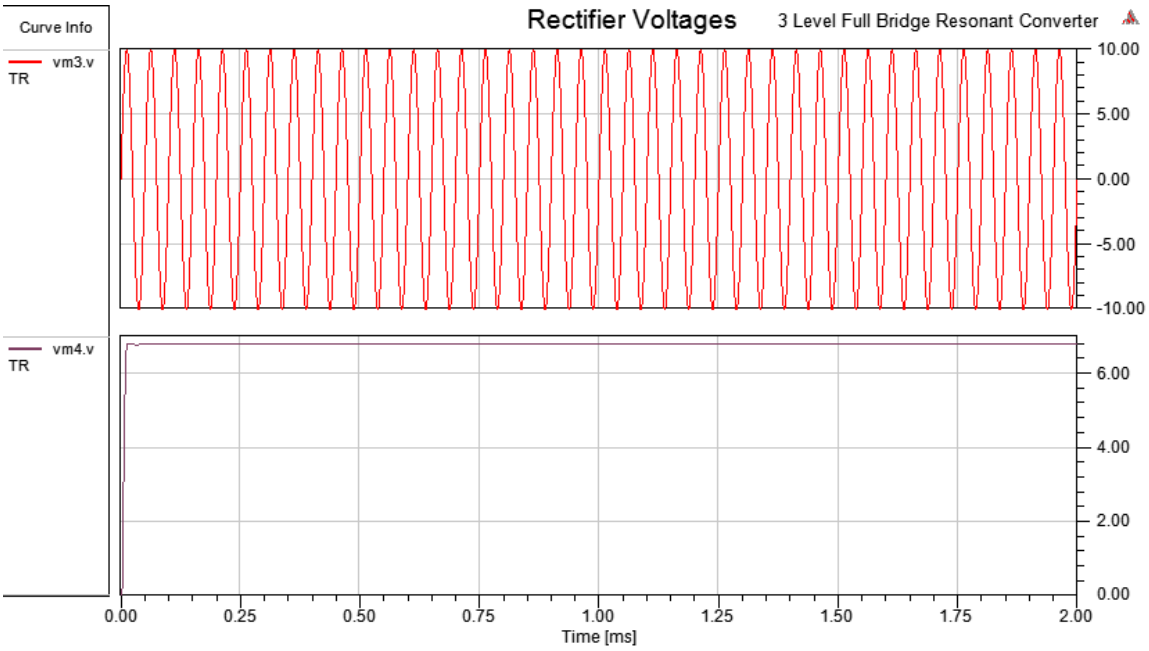


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

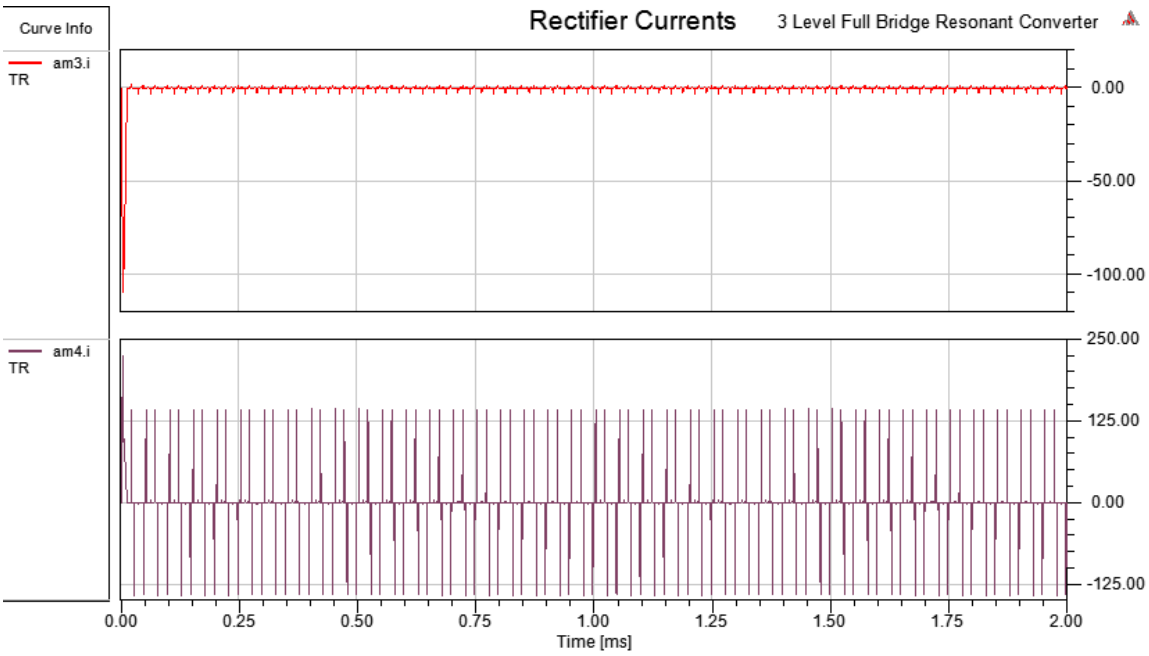


Figure 7: Rectifier Input/Output Currents

Load Three Level Full Bridge Resonant Converter Example

Three Level Half Bridge Resonant Converter Example

Description

The three levelhalf bridge resonant converter schematic is shown in Figure 1.

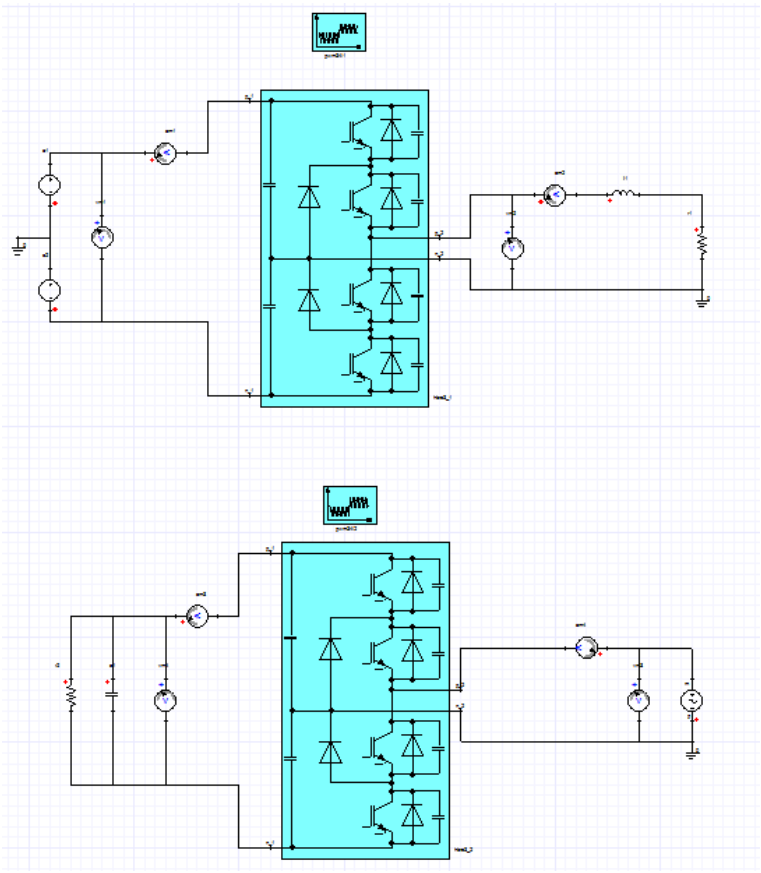


Figure 1: Three Level Half Bridge Resonant Converter Schematic

The system contains the pwm34i and hbrc3models from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 3 level half bridge resonant converter and the 3 level 4 pulse PWM generator in the Power System VHDL-AMS library.

hbrc3 can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the hbrc3 component as an inverter and the lower circuit shows the usage of the hbrc3 component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

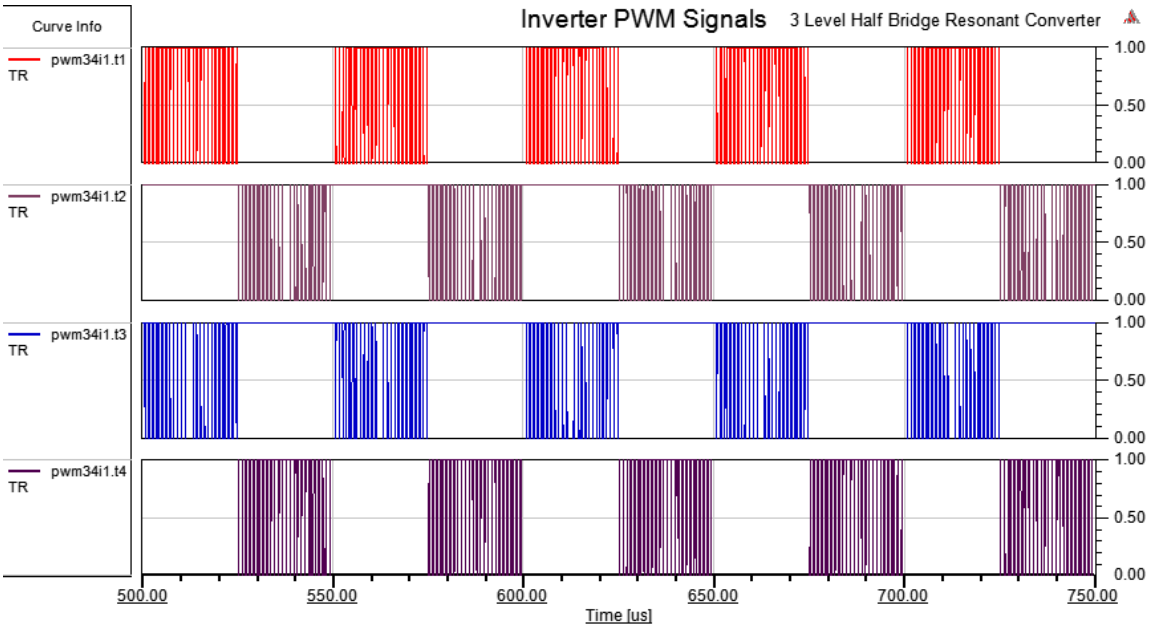


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

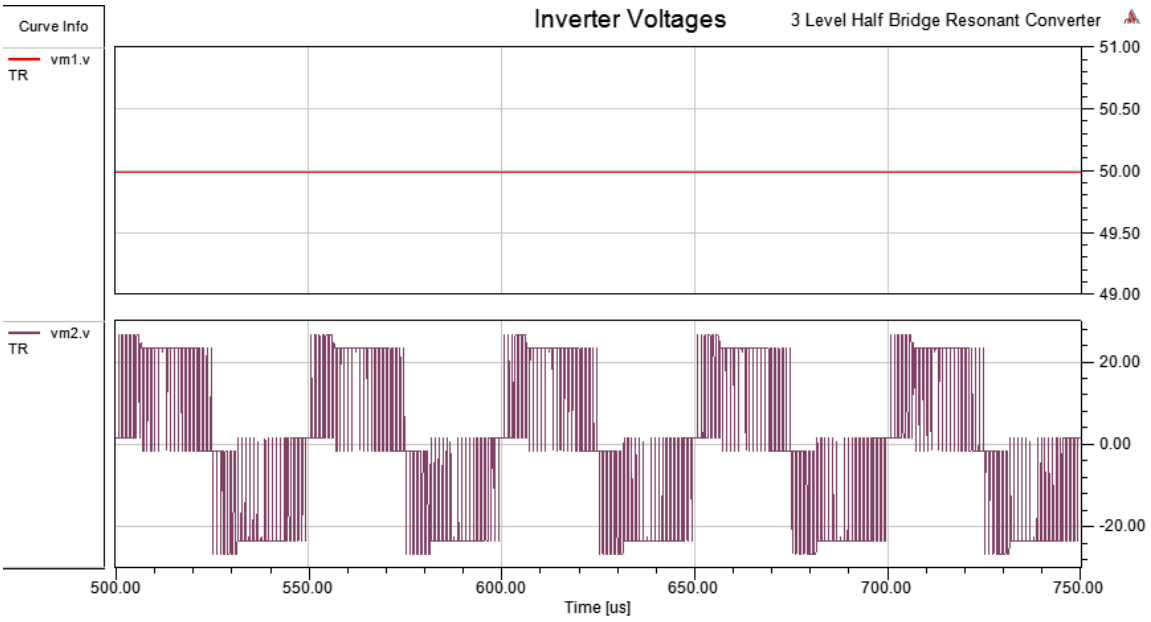


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

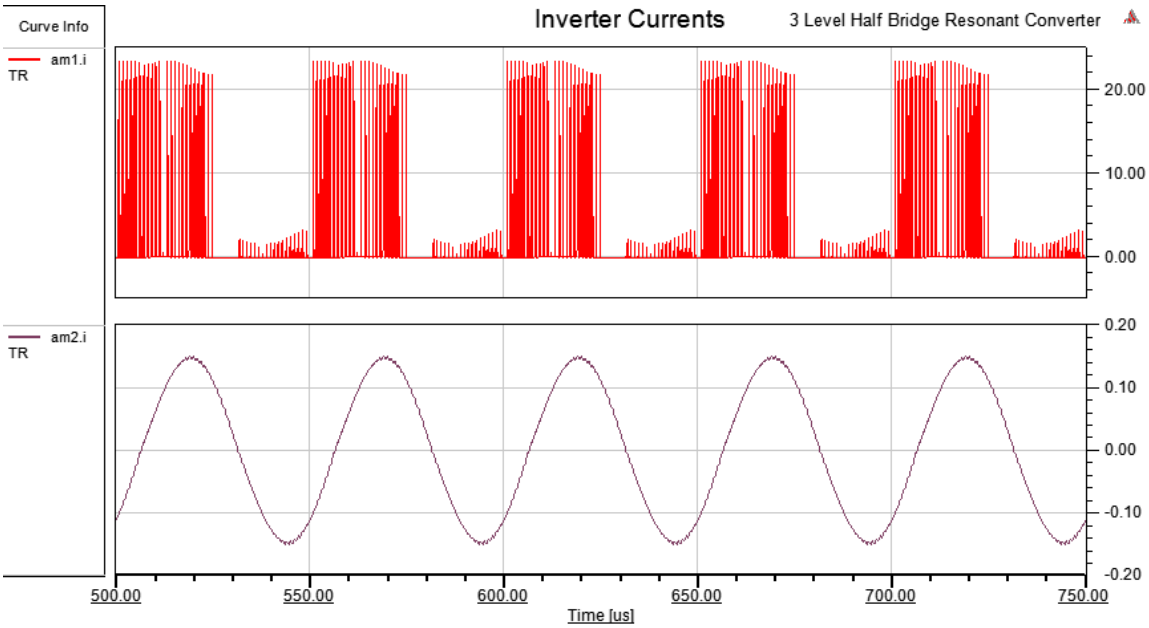


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

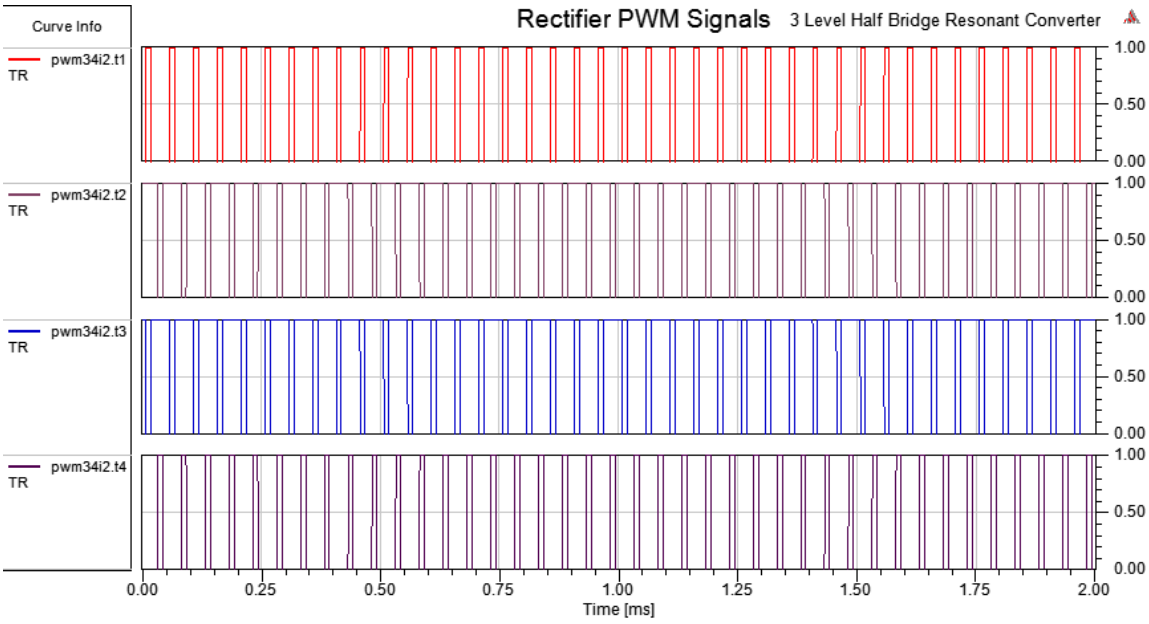


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

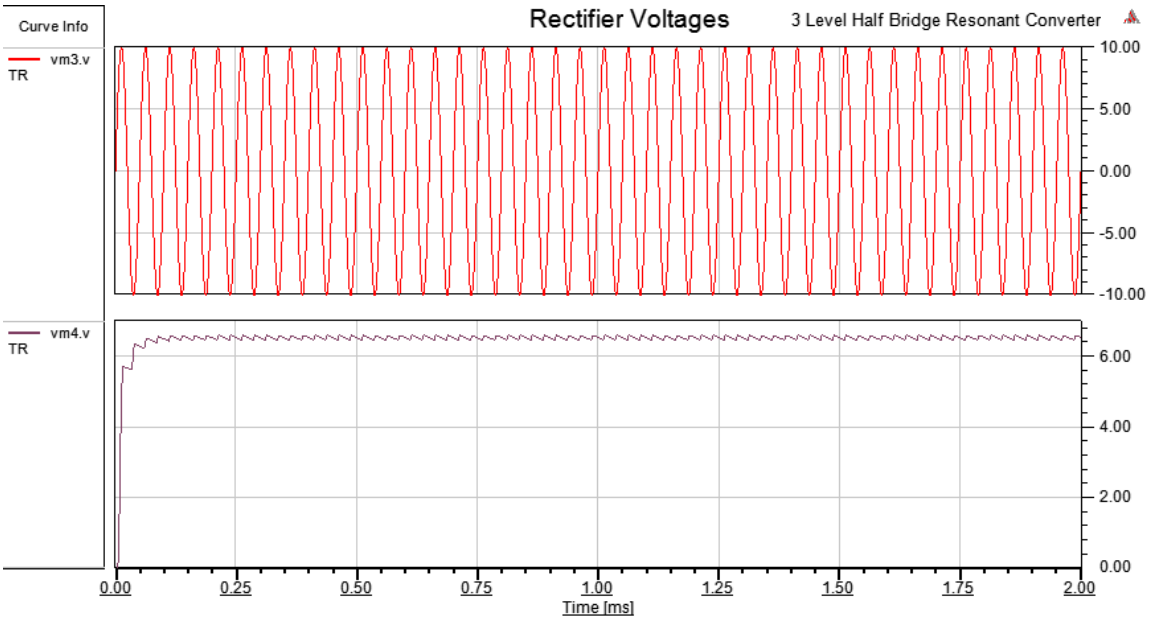


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

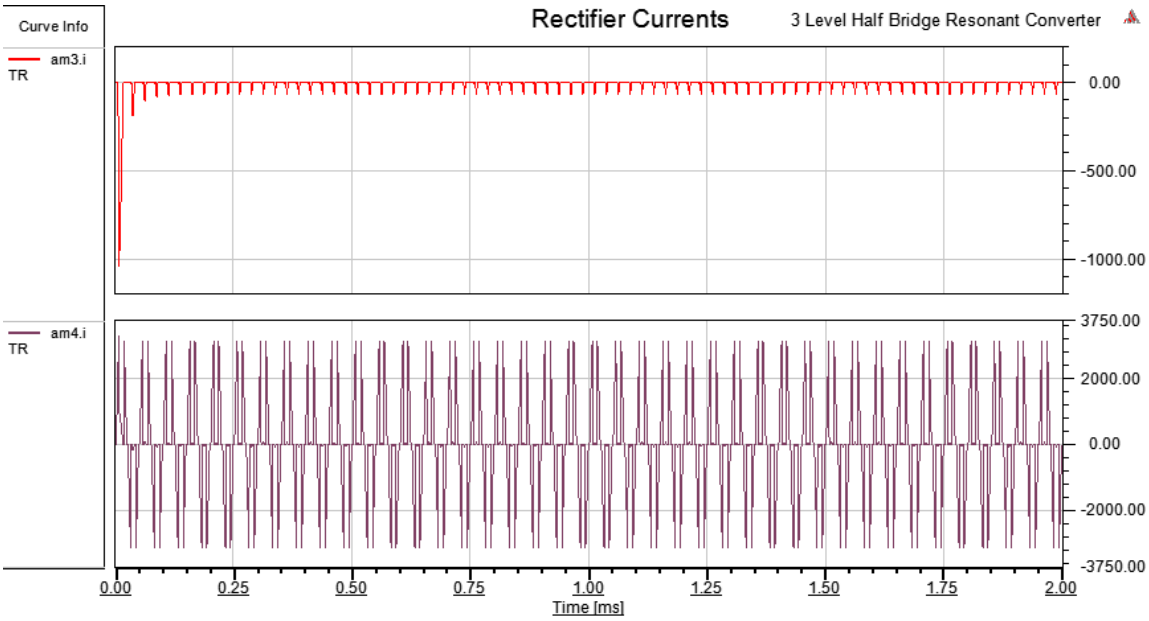


Figure 7: Rectifier Input/Output Currents

Load Three Level Half Bridge Resonant Converter Example

Three Level Three Phase Resonant Converter Example

Description

The three level three phase resonant converter schematic is shown in Figure 1.

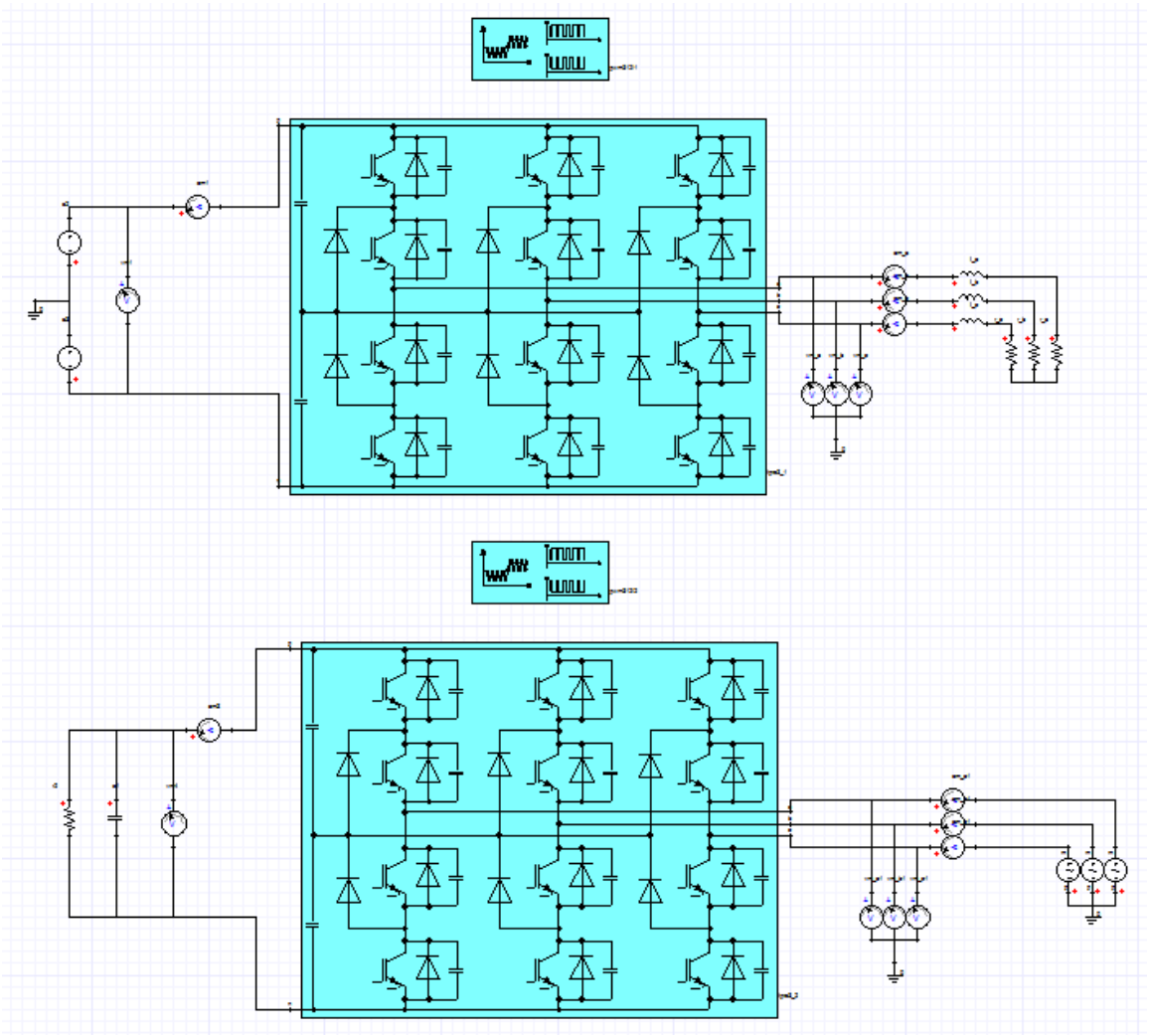


Figure 1: Three Level Three Phase Resonant Converter Schematic

The system contains the pwm312i and tprc3models from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 3 level three phase resonant converter and the 3 level 12 pulse PWM generator in the Power System VHDL-AMS library.

tprc3 can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the tprc3 component as an inverter and the lower circuit shows the usage of the tprc3 component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

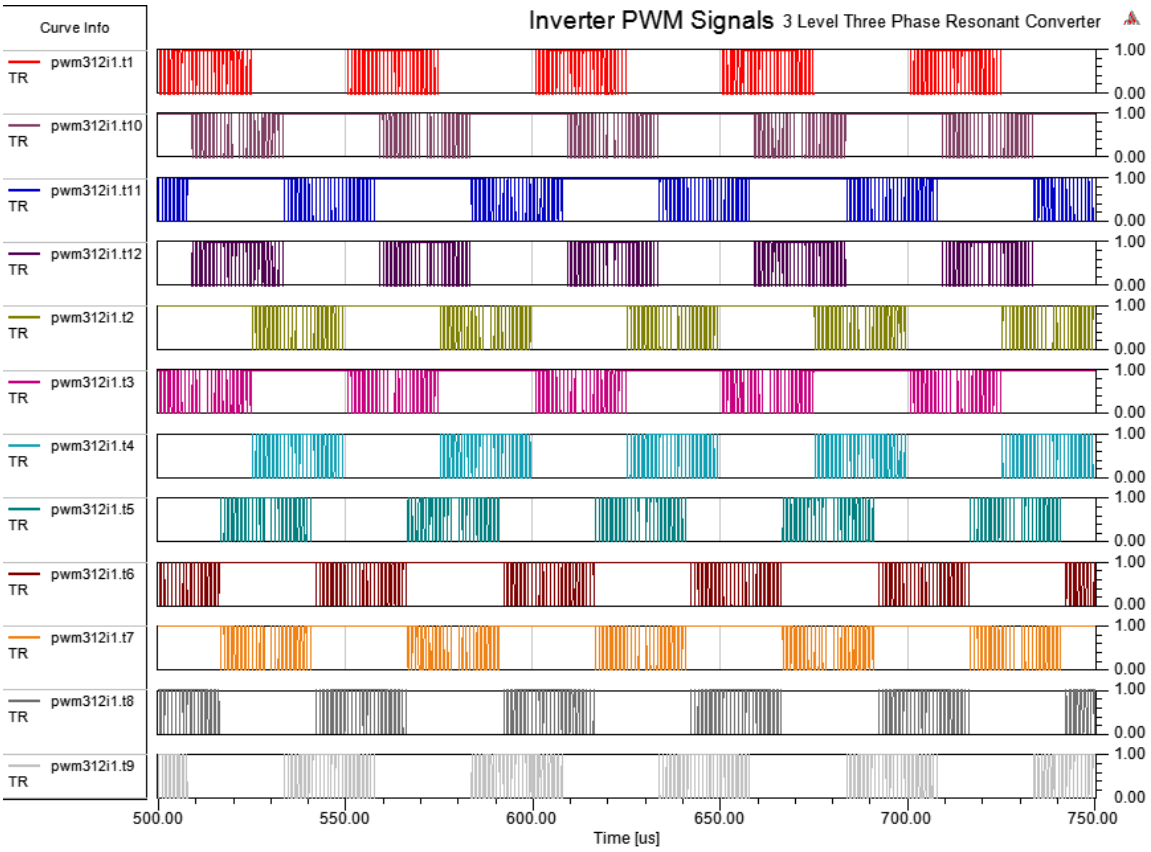


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

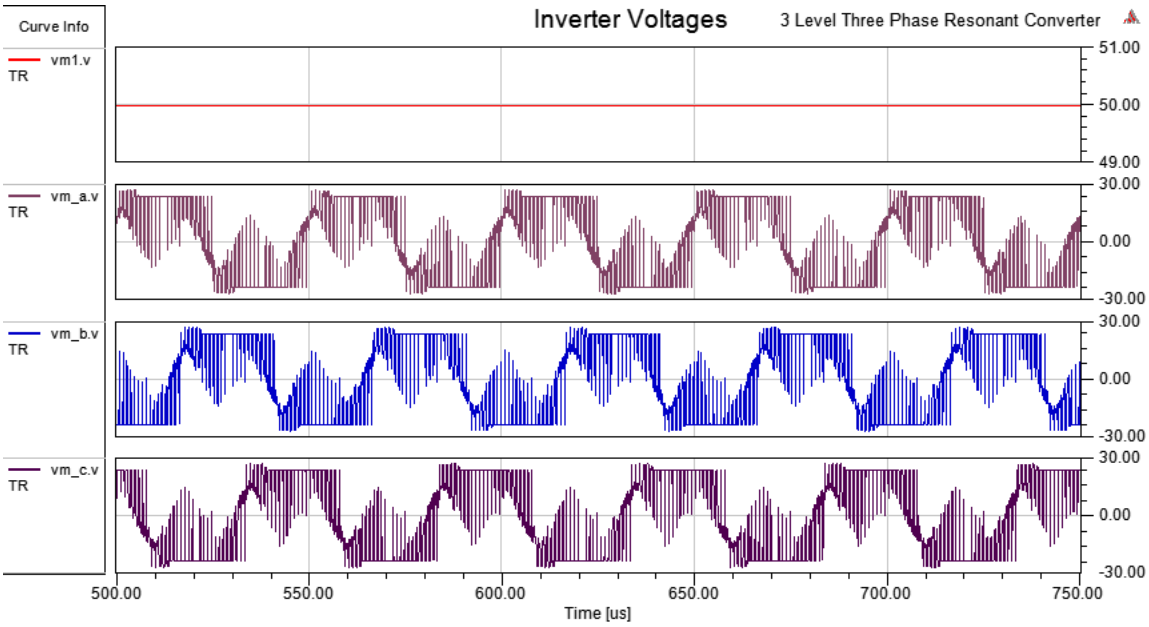


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

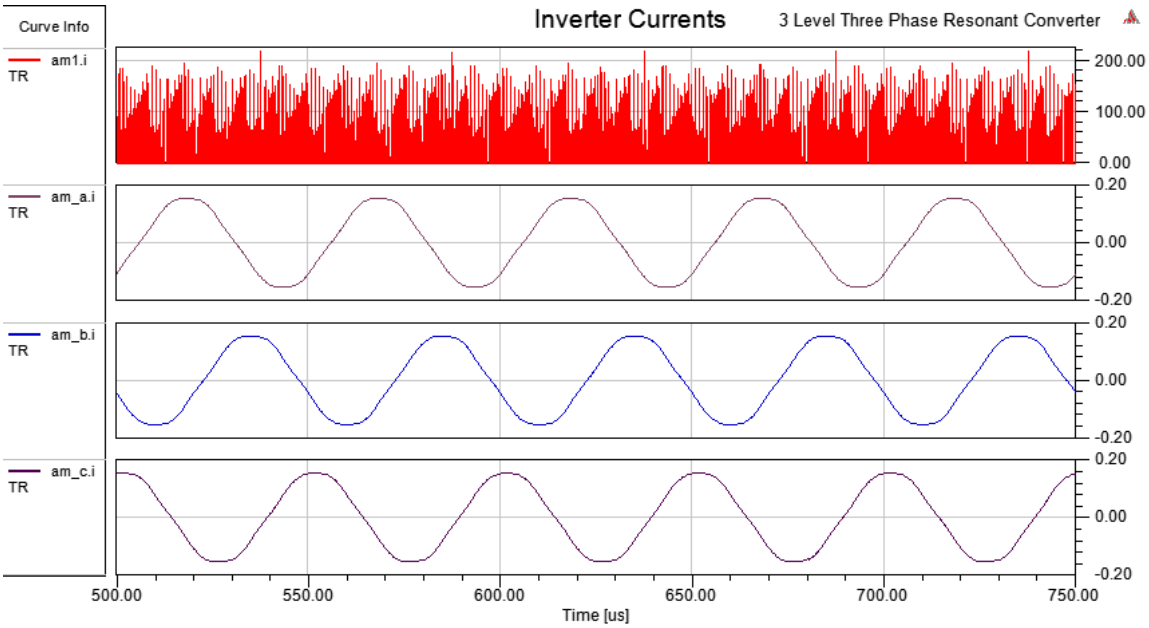


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

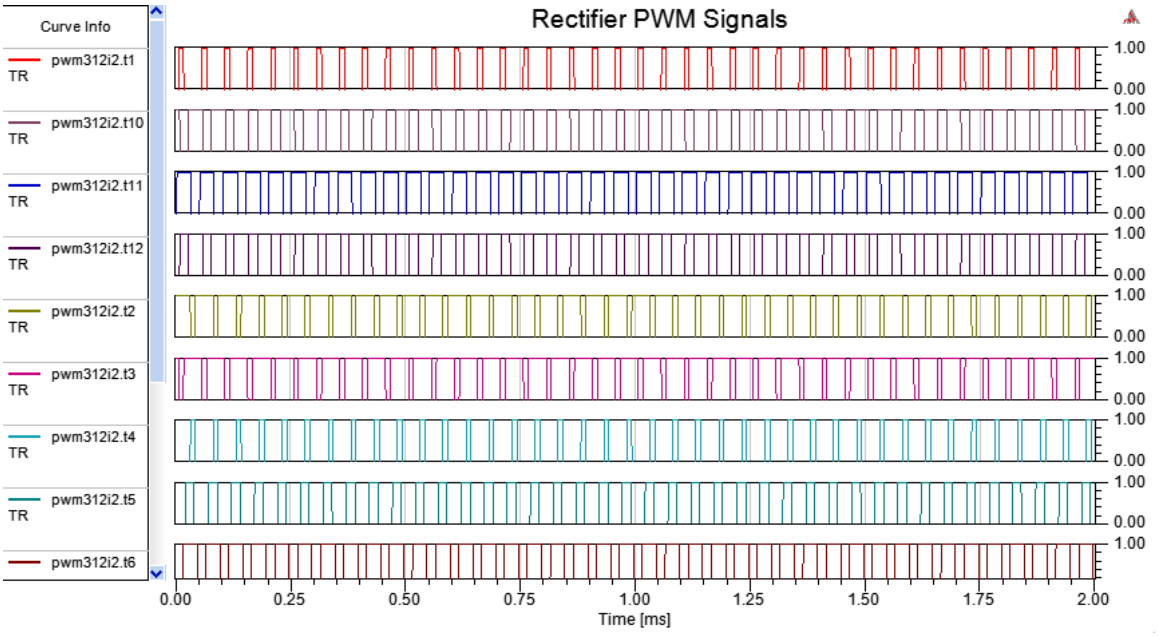


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

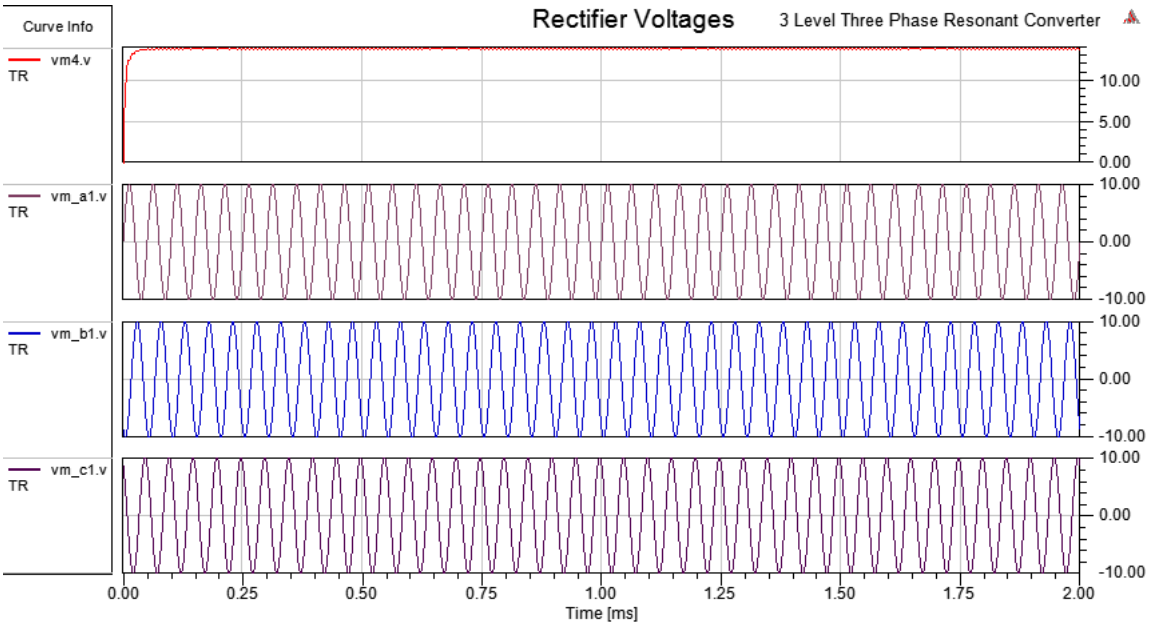


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

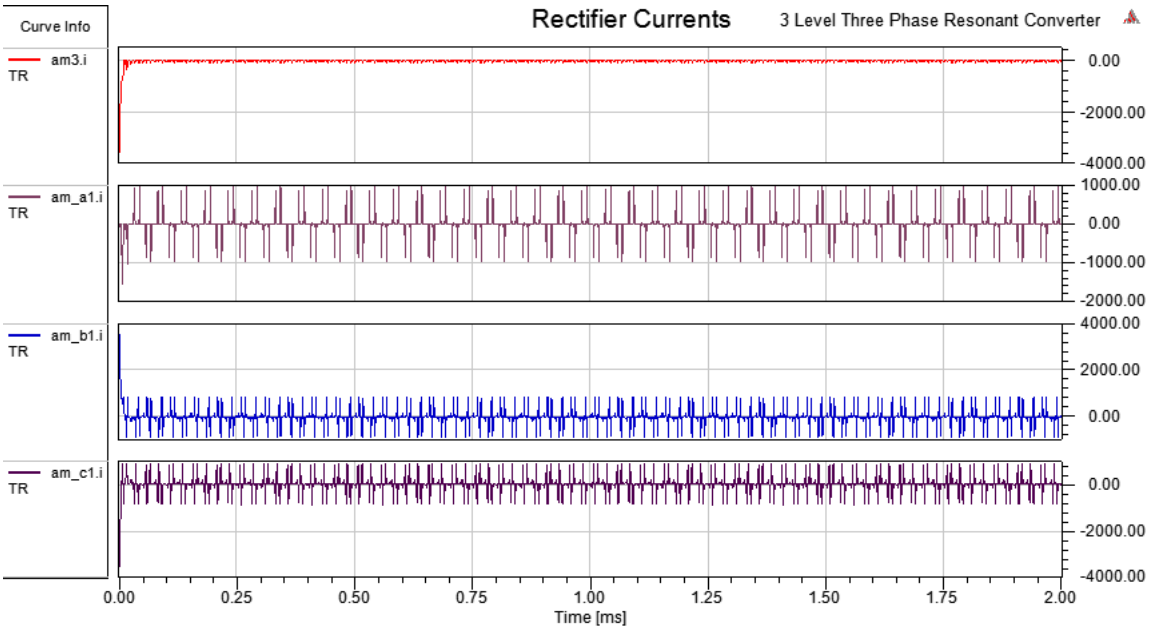


Figure 7: Rectifier Input/Output Currents

Three Level Twelve Pulse PWM Example

Description

The three level twelve pulse PWM schematic is shown in Figure 1.

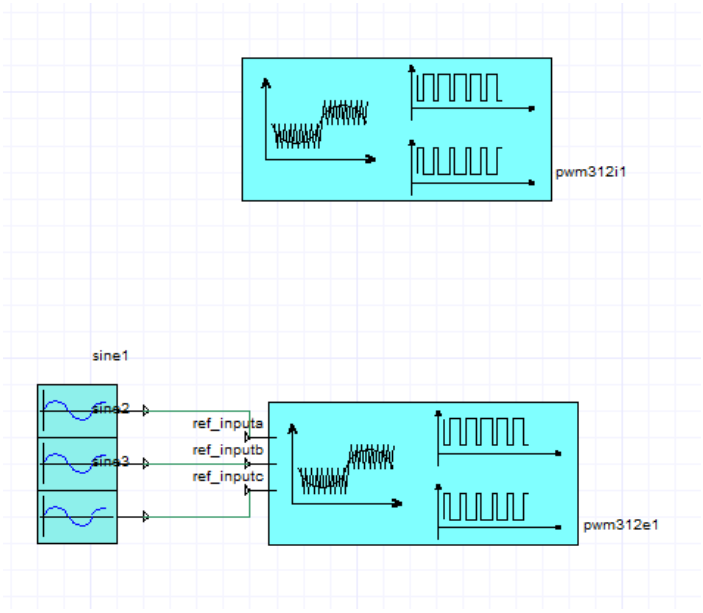


Figure 1: Three Level Twelve Pulse PWM Schematic

The system contains the pwm312i and pwm312emodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of three level twelve pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The control signalsgenerated from pwm312i are shown in Figure 2.

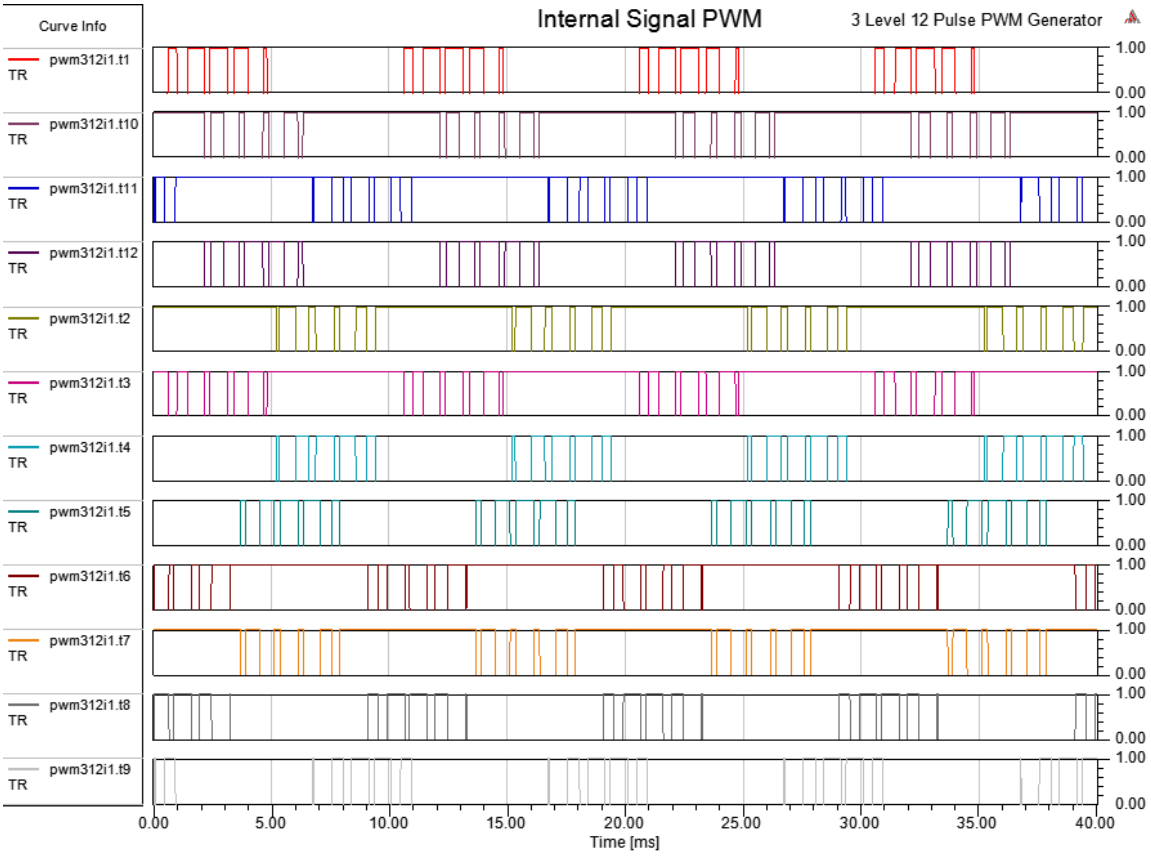


Figure 2: Internal Signal PWM

The control signals generated from pwm312e are shown in Figure 3.

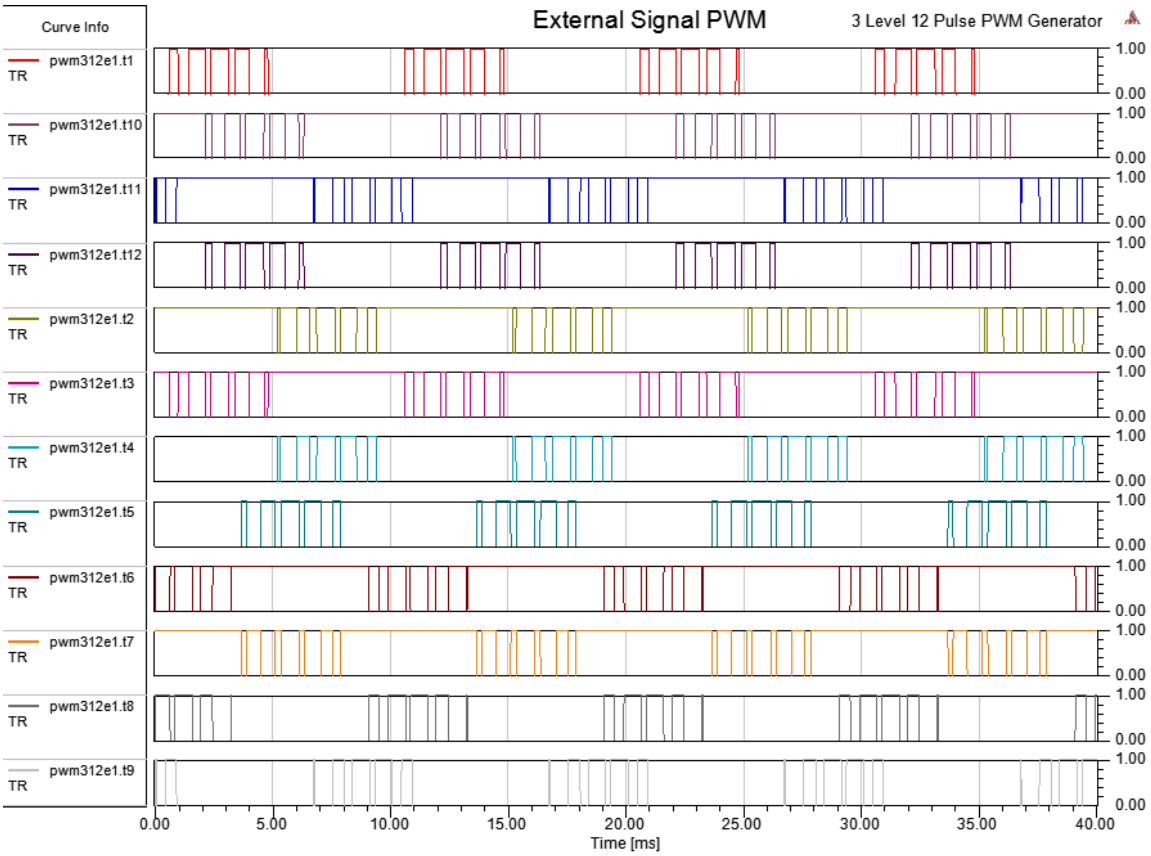


Figure 3: External Signal PWM

Three Phase Resonant Converter Example

Description

The three phase resonant converter schematic is shown in Figure 1.

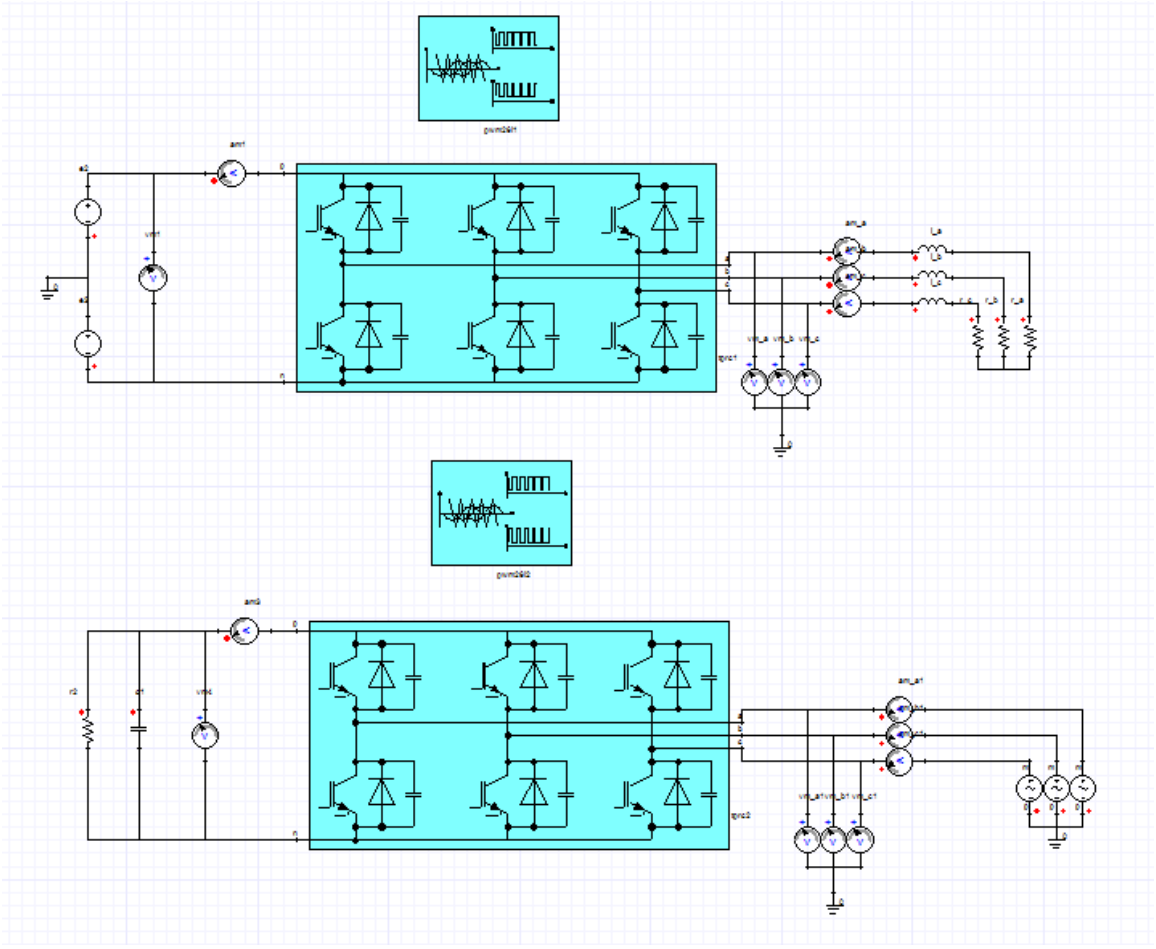


Figure 1: Three Phase Resonant Converter Schematic

The system contains the pwm26i and tprcmodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of the 2 level three phase resonant converter and the 2 level 6 pulse PWM generator in the Power System VHDL-AMS library.

tprc can be used as inverter or rectifier, it is based on the design setting and the PWM signal generation setting. In the example schematic, the upper circuit shows the usage of the tprc component as an inverter and the lower circuit shows the usage of the tprc component as a rectifier.

The results are shown below.

Simulation Results

The PWM signals generated for the inverter from 500us to 750us are shown in Figure 2.

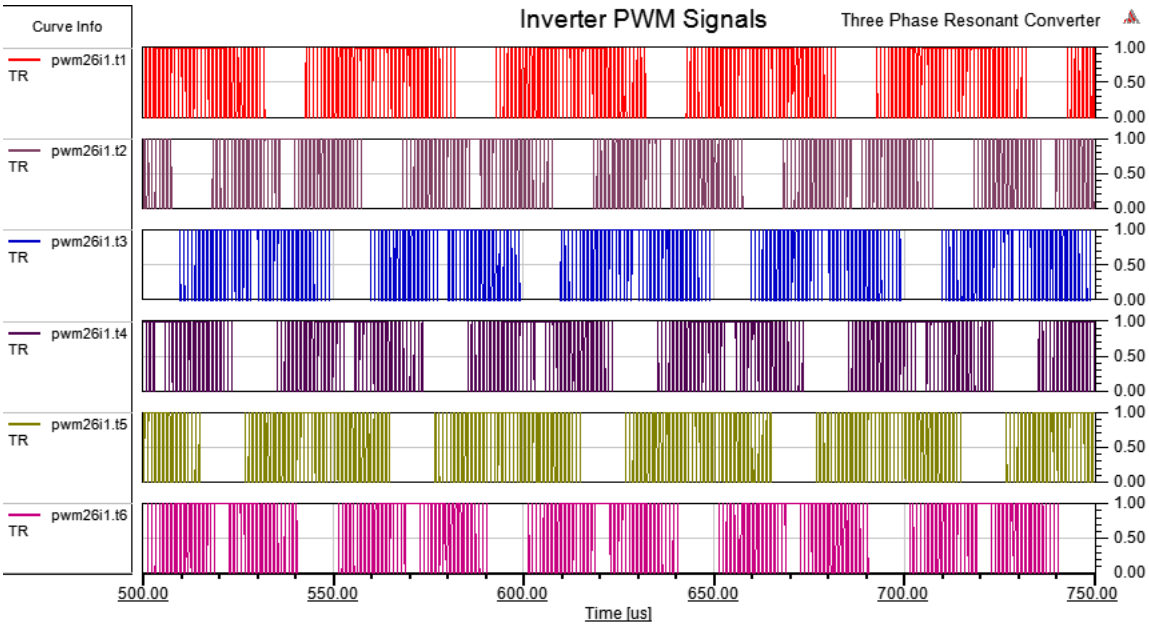


Figure 2: Inverter PWM Signals

The Inverter Input/Output voltages from 500us to 750us are shown in Figure 3.

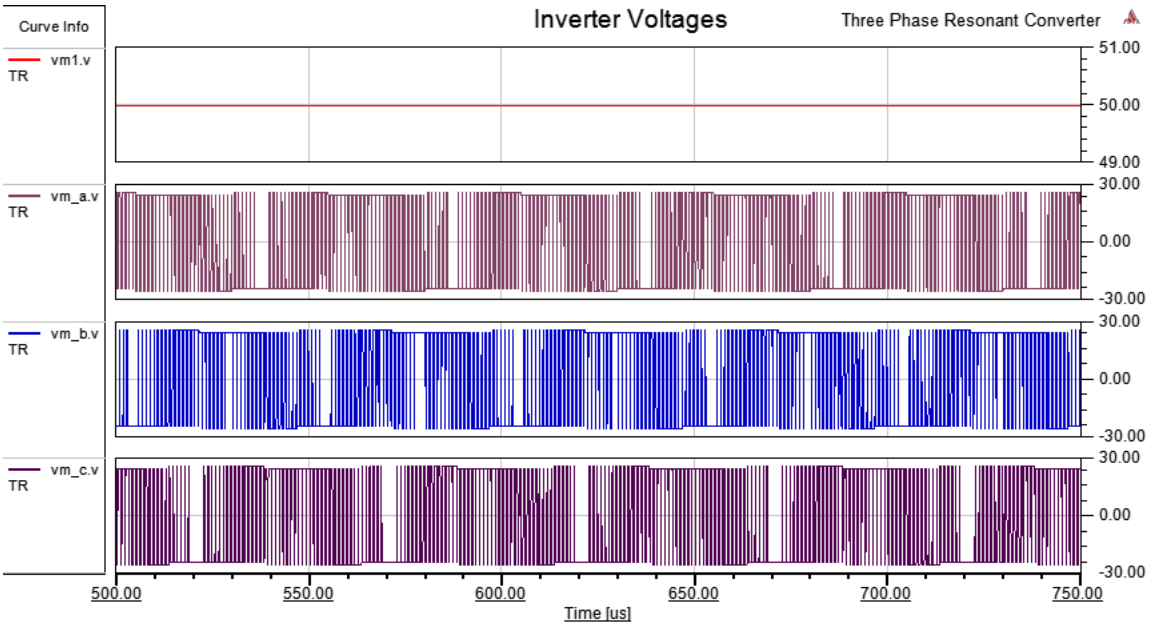


Figure 3: Inverter Input/Output Voltages

The Inverter Input/Output currents from 500us to 750us are shown in Figure 4.

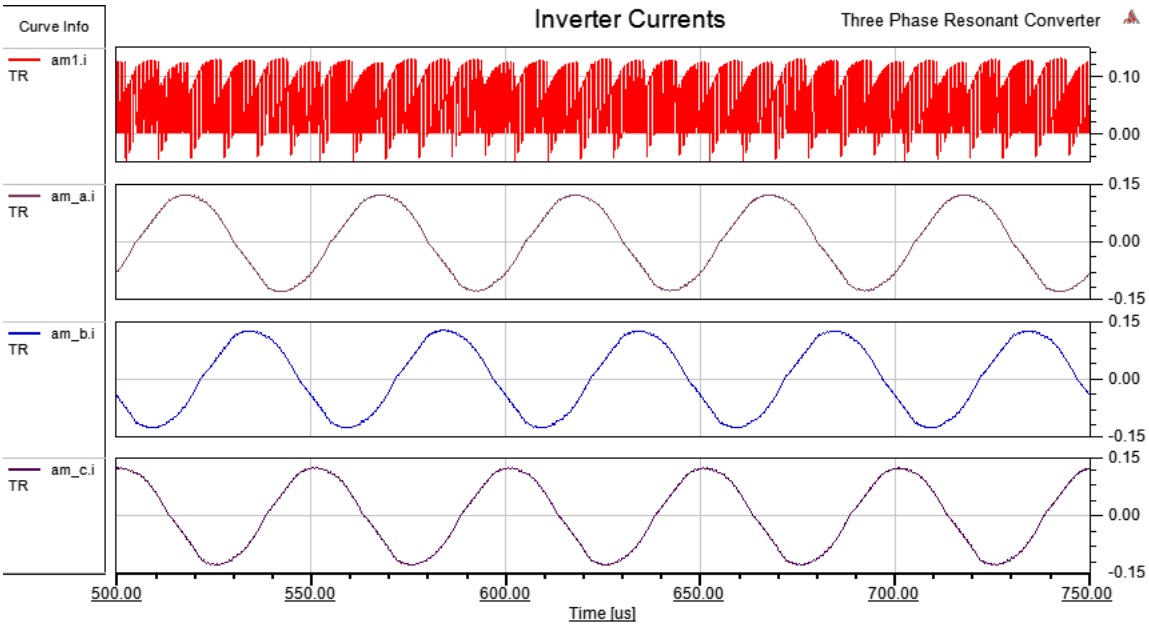


Figure 4: Inverter Input/Output Currents

The PWM signals generated for the rectifier are shown in Figure 5.

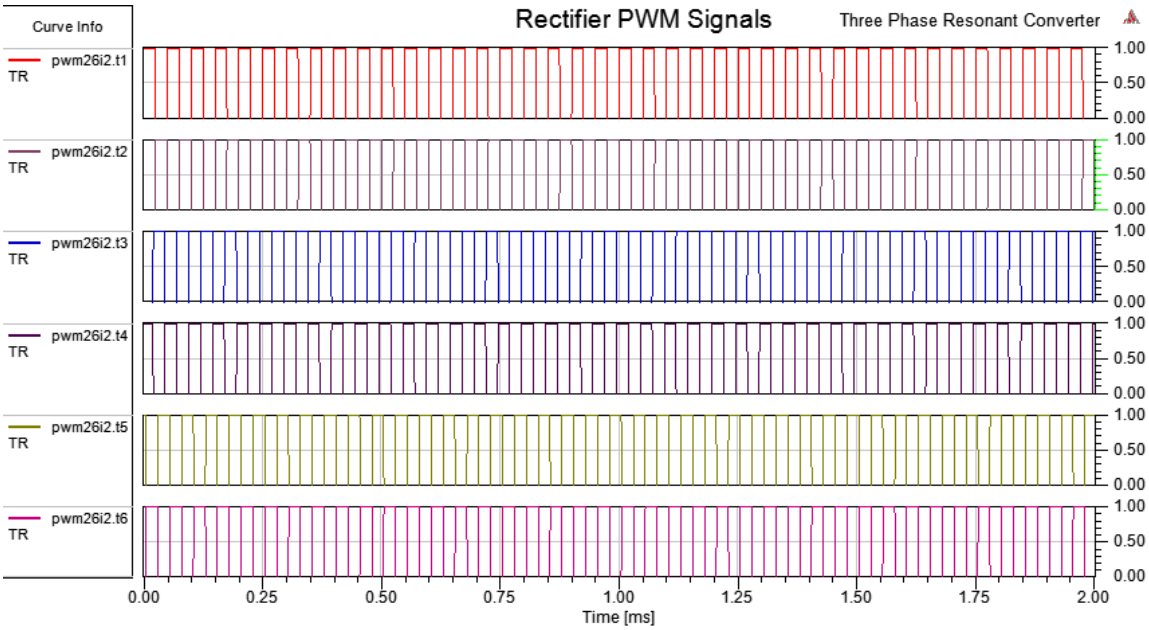


Figure 5: Rectifier PWM Signals

The rectifier Input/Output voltages are shown in Figure 6.

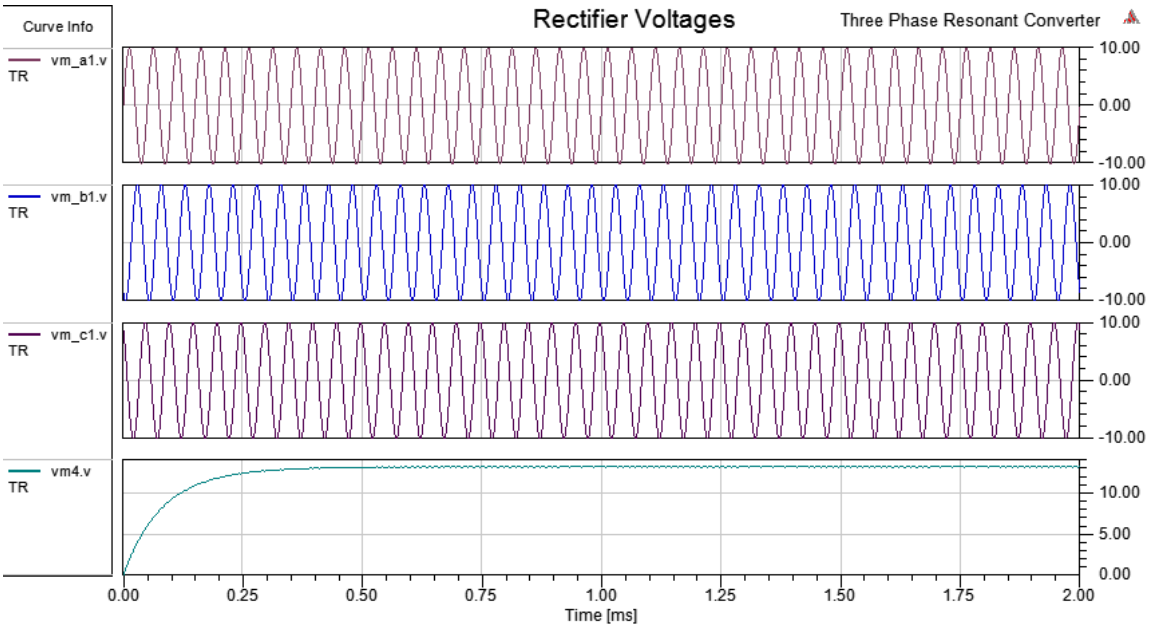


Figure 6: Rectifier Input/Output Voltages

The rectifier Input/Output currents are shown in Figure 7.

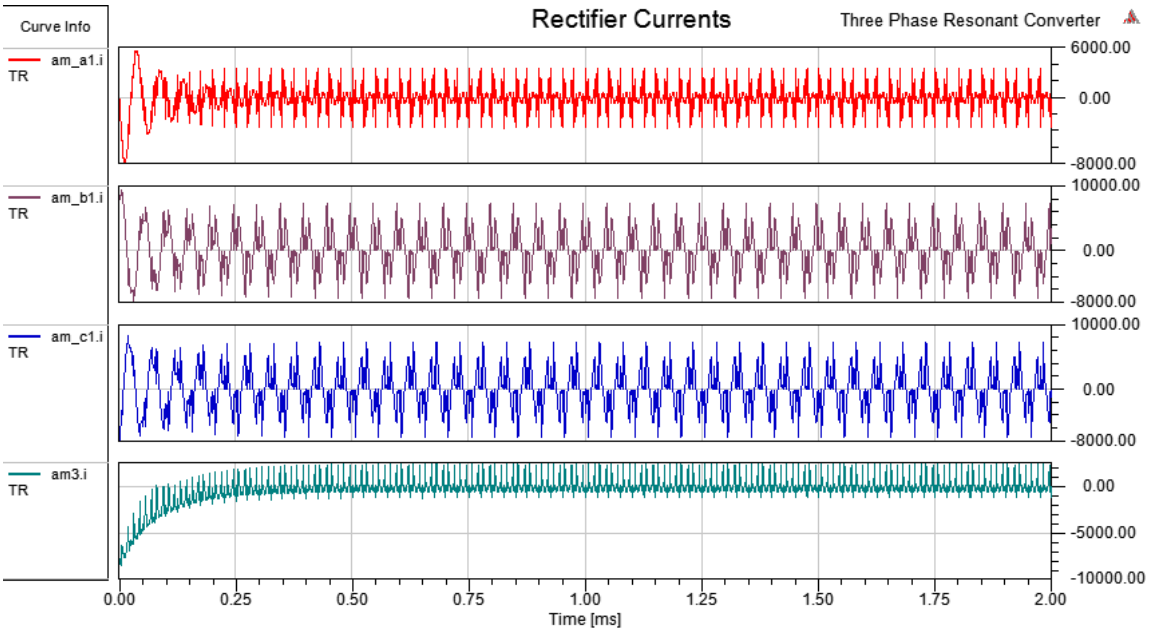


Figure 7: Rectifier Input/Output Currents

Load Three Phase Resonant Converter Example

Translational Electromechanical Converter Example

Description

The translational electromechanical converter schematic is shown in Figure 1.

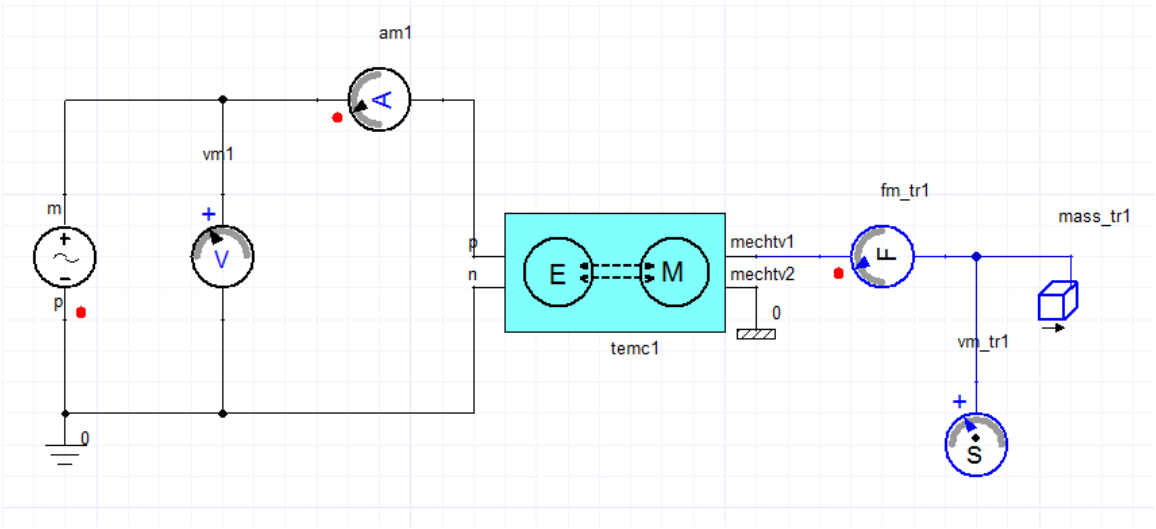


Figure 1: Translational Electromechanical ConverterSchematic

The system contains thetemc model from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage oftranslational electromechanical converter in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The electrical quantities are shown in Figure 2.

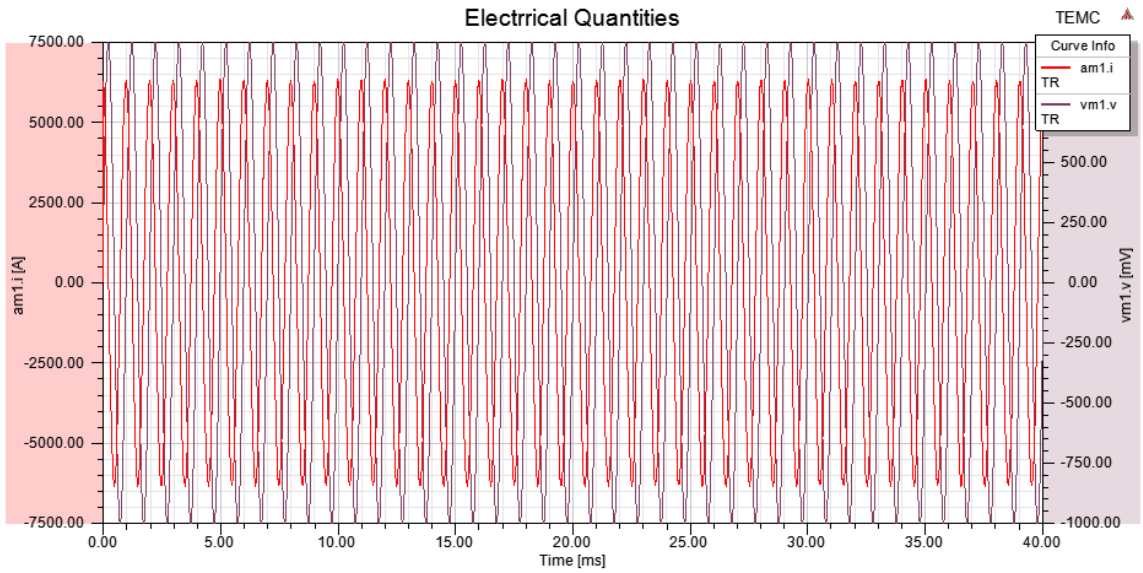


Figure 2: Electrical Quantities

The mechanical quantities are shown in Figure 3.

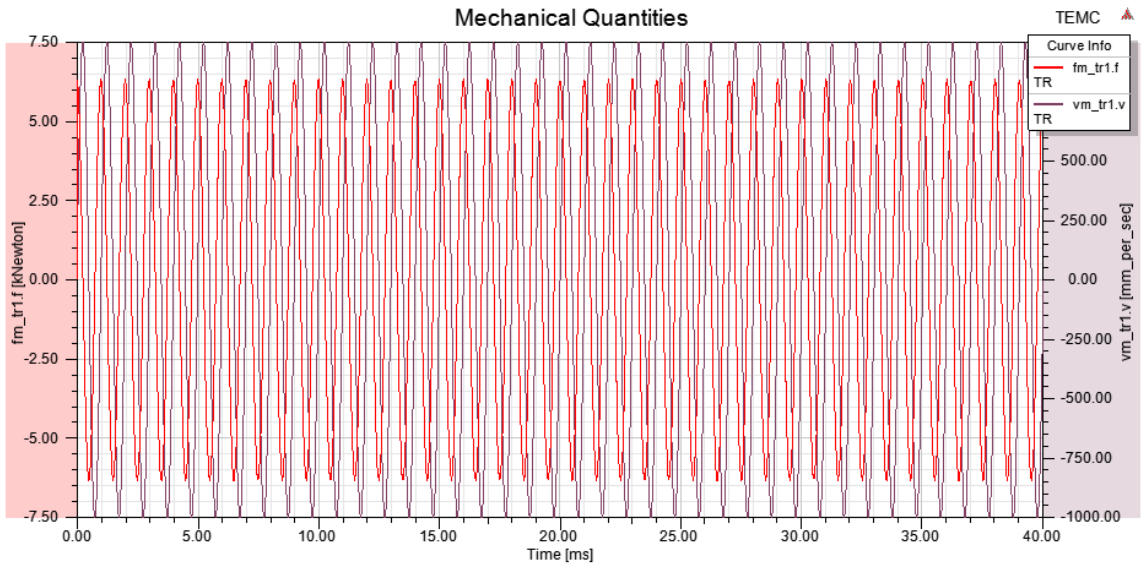


Figure 3: Mechanical Quantities

The power comparison isshown in Figure 4.

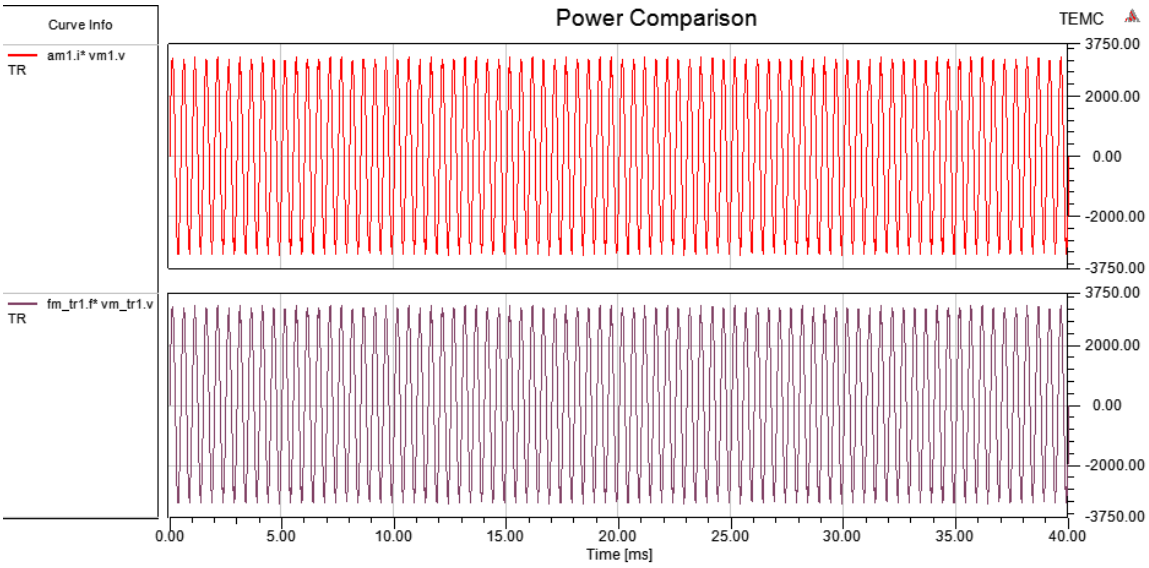


Figure 4: Power Comparison

Transmission Line Long Single Phase Example

Description

The transmission line long single phase schematic is shown in Figure 1.

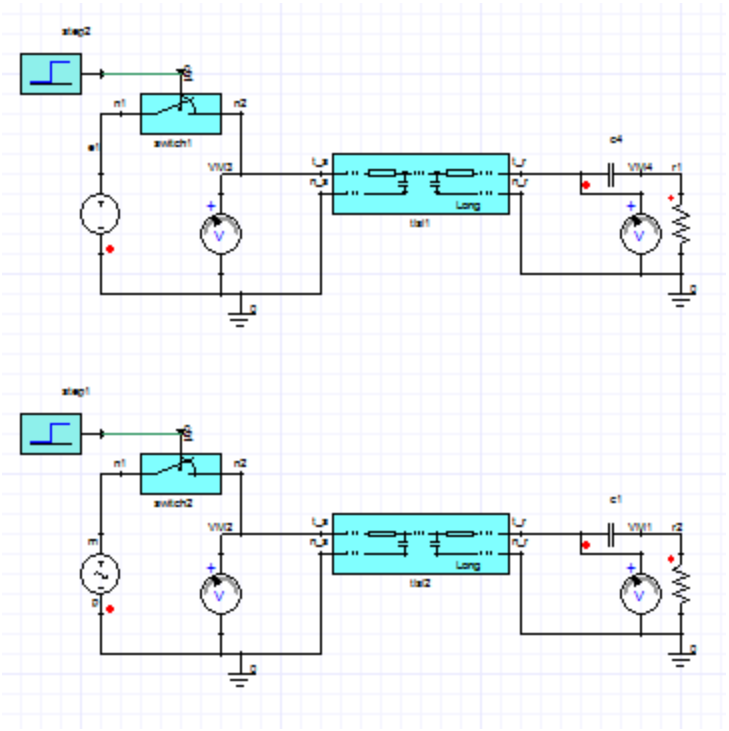


Figure 1: Transmission Line Long Single PhaseSegmentSchematic

The system contains thetlsl and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofsingle phase long transmission line component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The DC voltages comparison is shown in Figure 2.

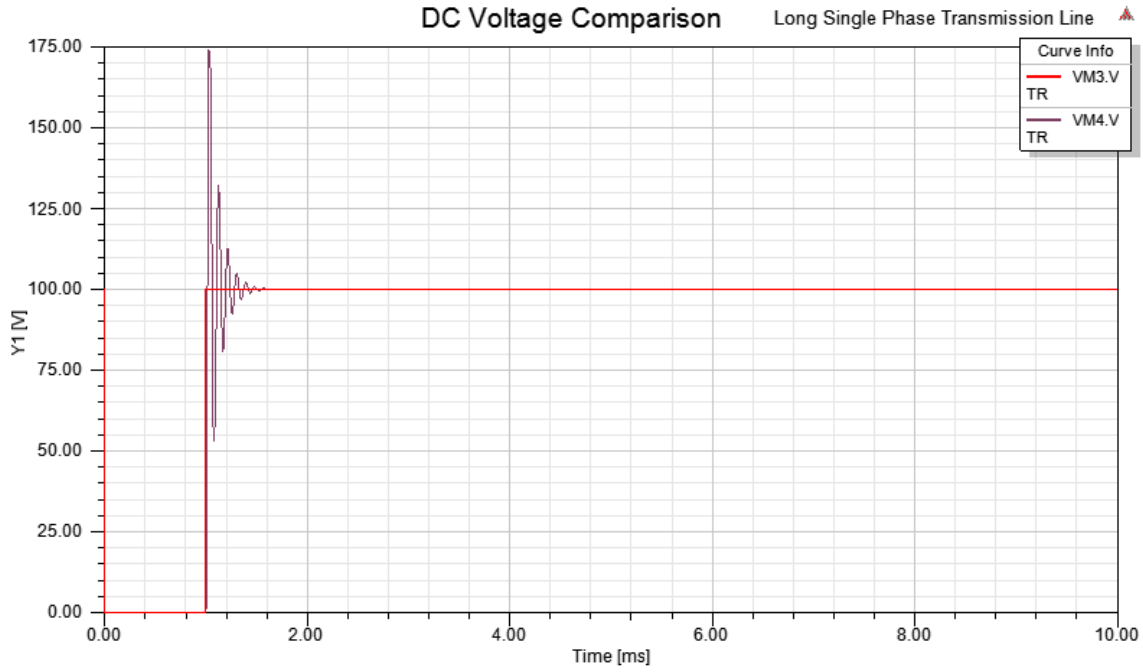


Figure 2: DC Voltage Comparison

The AC voltages comparison is shown in Figure 3.

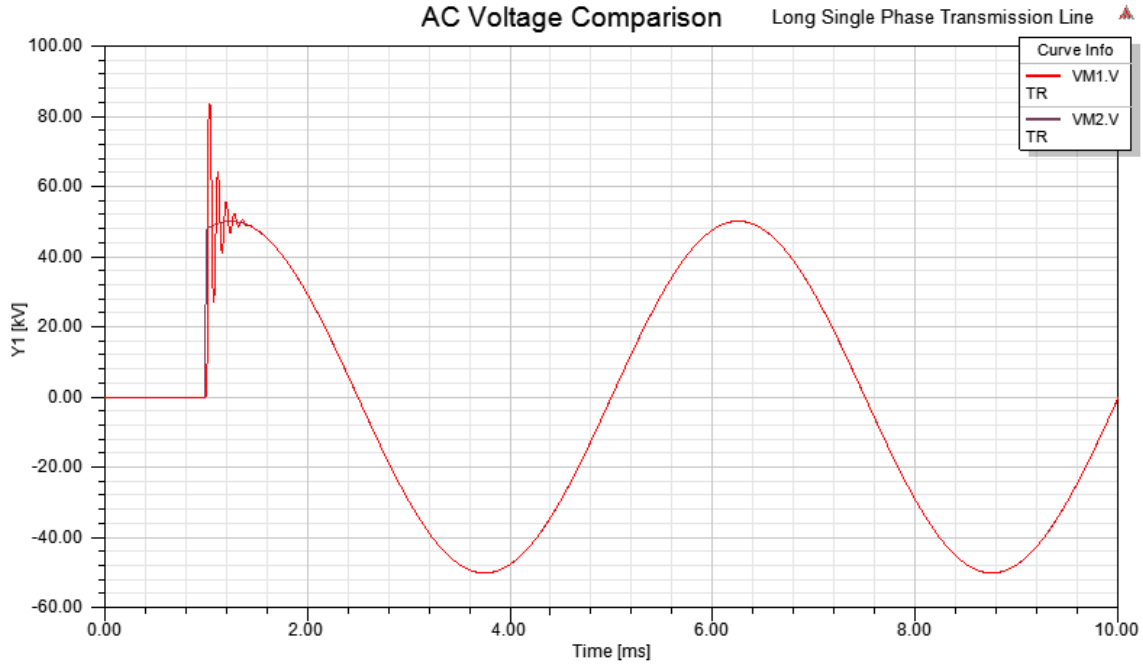


Figure 3: AC Voltage Comparison

Transmission Line Long Single Phase Segment Example

Description

The transmission line long single phasesegmentschematic is shown in Figure 1.

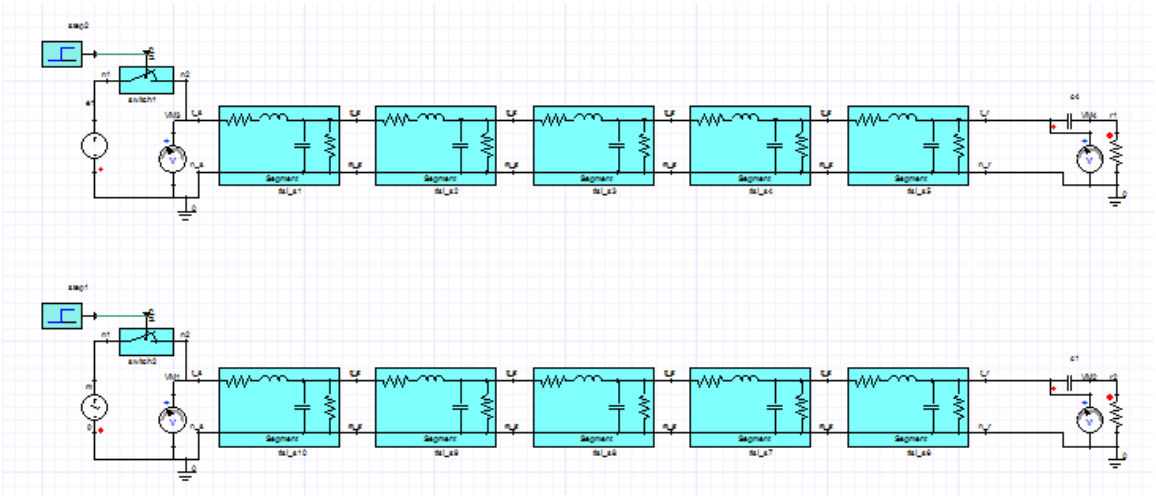


Figure 1: Transmission Line Long Single PhaseSegmentSchematic

The system contains thetlsl_s and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofsingle phase long transmission line segment component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The DC voltages comparison is shown in Figure 2.

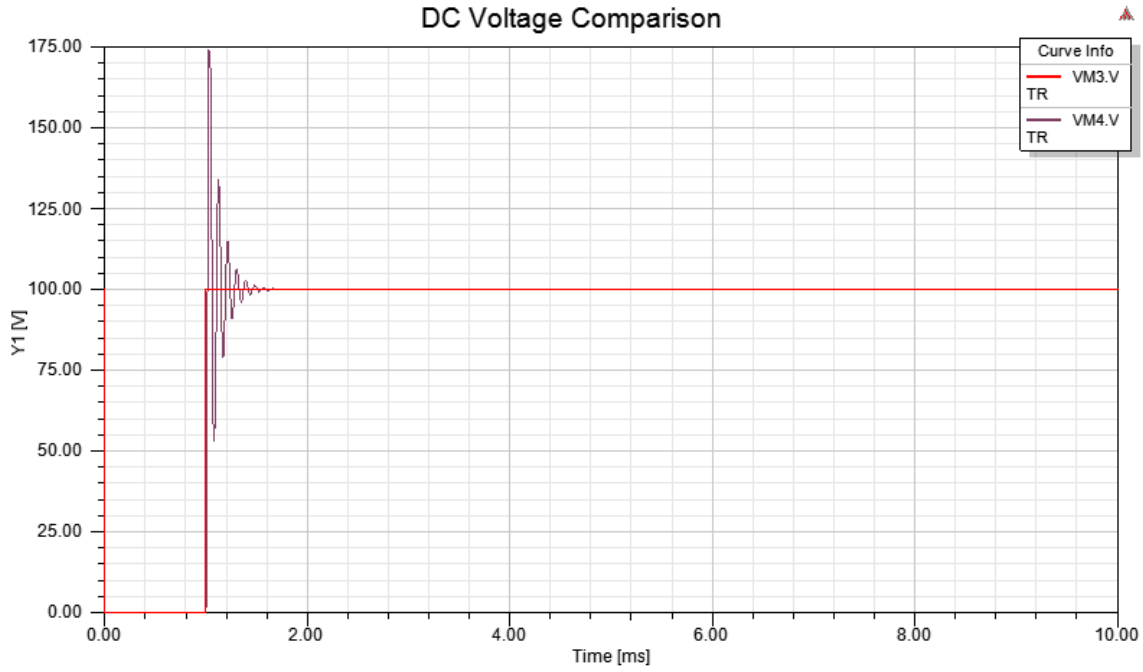


Figure 2: DC Voltage Comparison

The AC voltages comparison is shown in Figure 3.

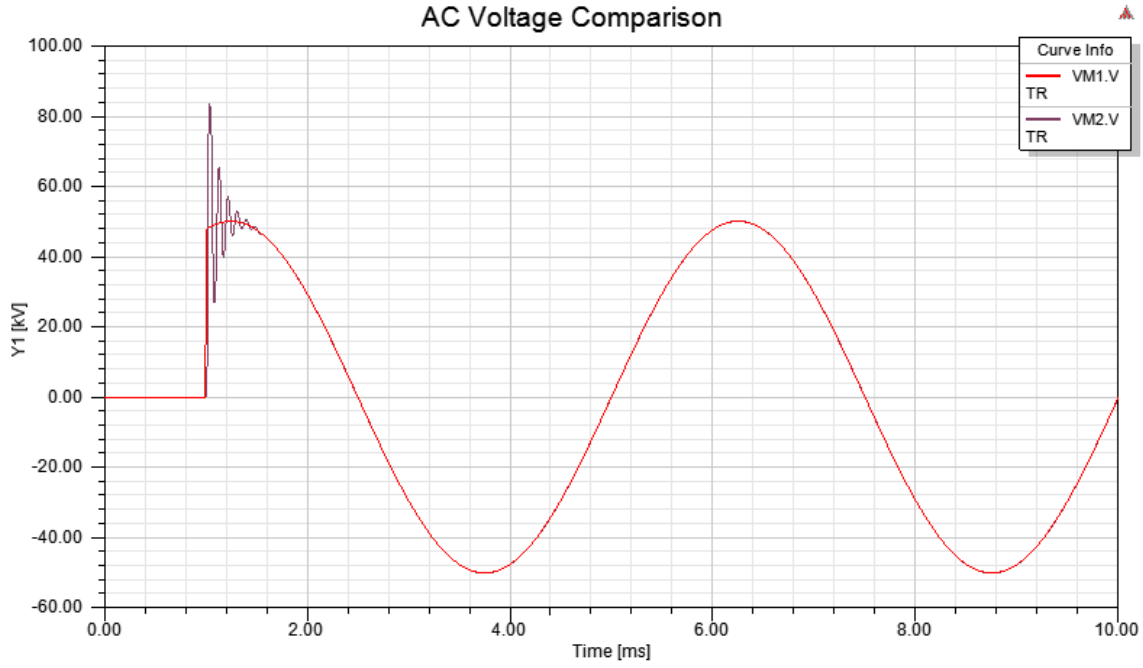


Figure 3: AC Voltage Comparison

Load Transmission Line Long Single Phase Segment Example

Transmission Line Long Three Phase Example

Description

The transmission line long three phase schematic is shown in Figure 1.

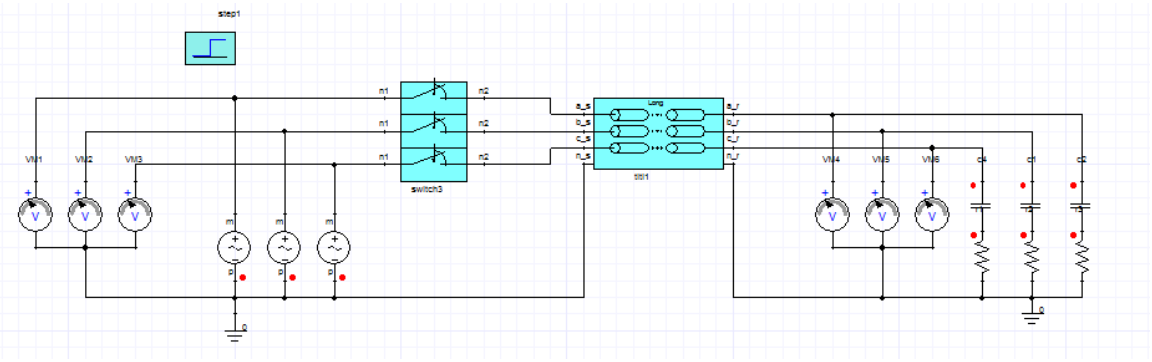


Figure 1: Transmission Line Long Three PhaseSchematic

The system contains thetltl and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofthree phase long transmission line component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The source voltages are shown in Figure 2.

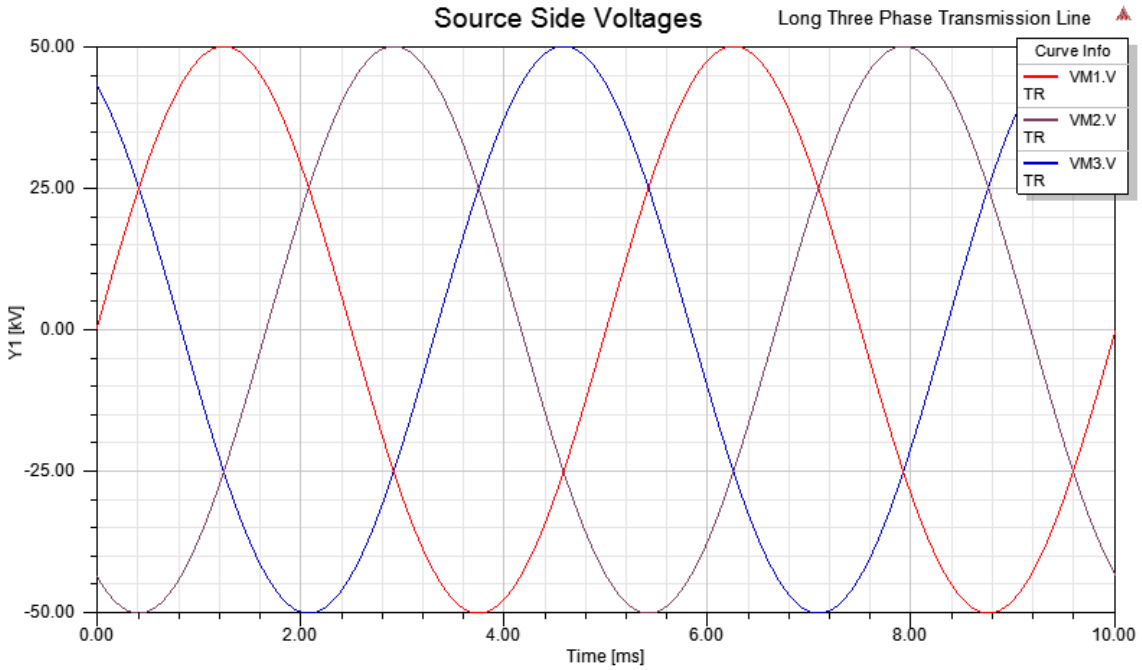


Figure 2: Source Voltages

The load voltages are shown in Figure 3.

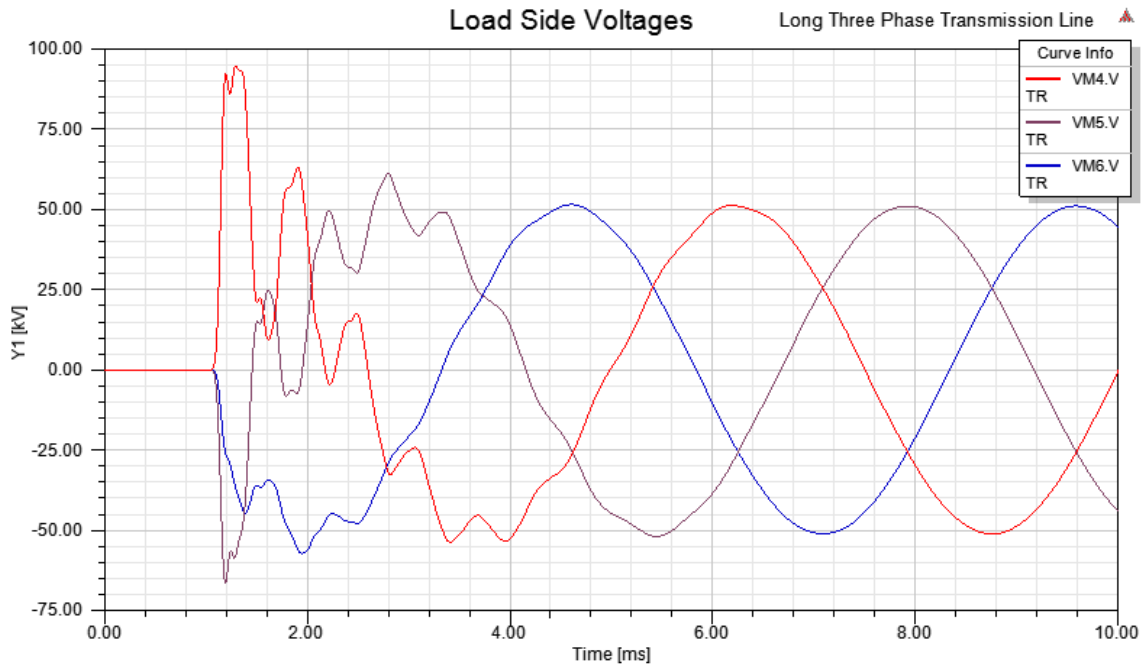


Figure 3: Load Voltages

The source/load voltages comparison is shown in Figure 4.

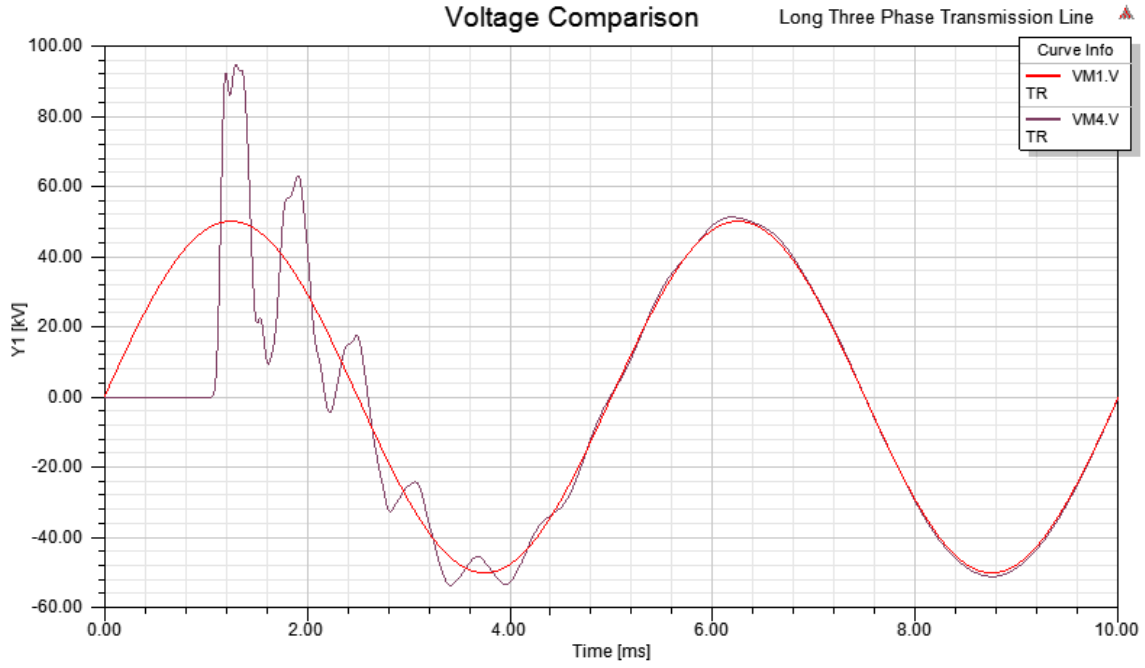


Figure 4: Source/Load Voltages Comparison

Transmission Line Long Three Phase Segment Example

Description

The transmission line long three phase segment schematic is shown in Figure 1.

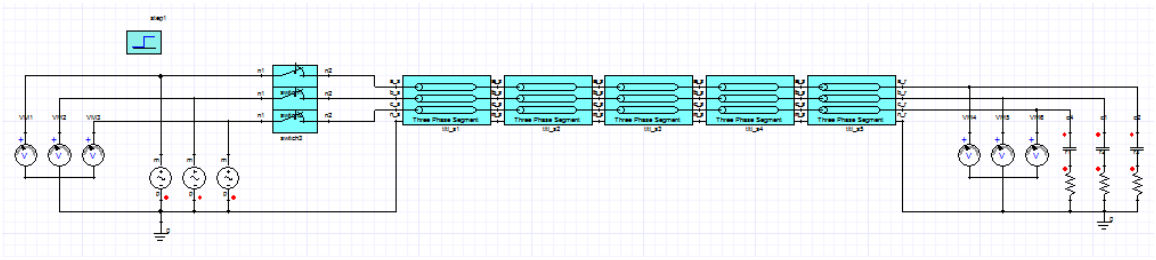


Figure 1: Transmission Line Long Three Phase SegmentSchematic

The system contains thetltl_s and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofthree phase long transmission line segment component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The source voltages are shown in Figure 2.

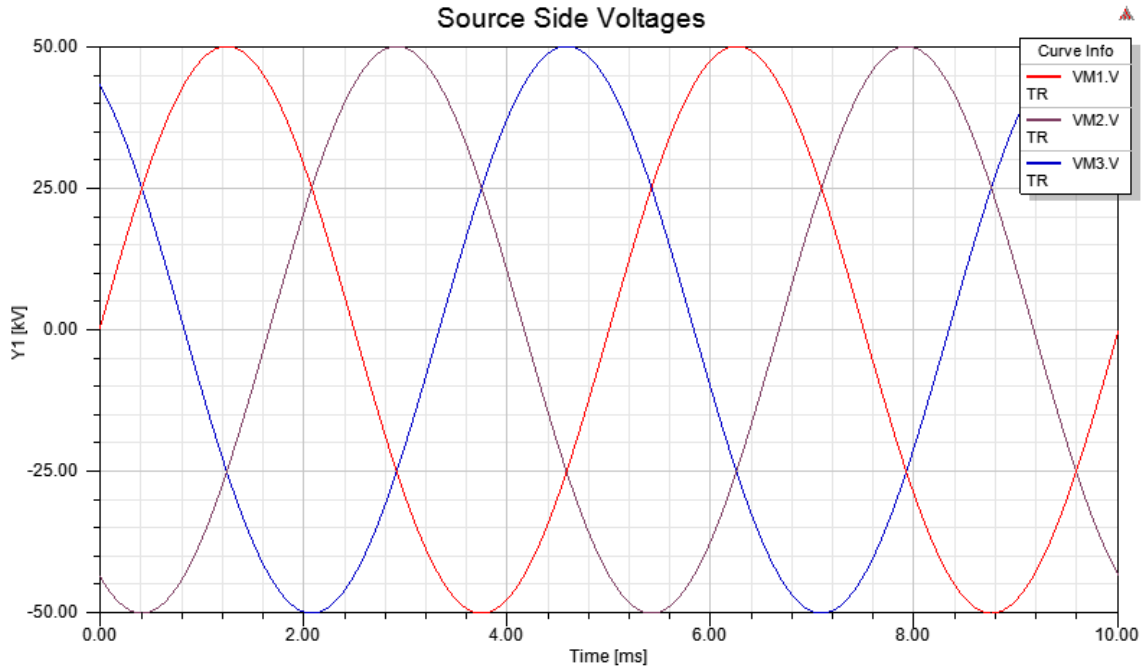


Figure 2: Source Voltages

The load voltages are shown in Figure 3.

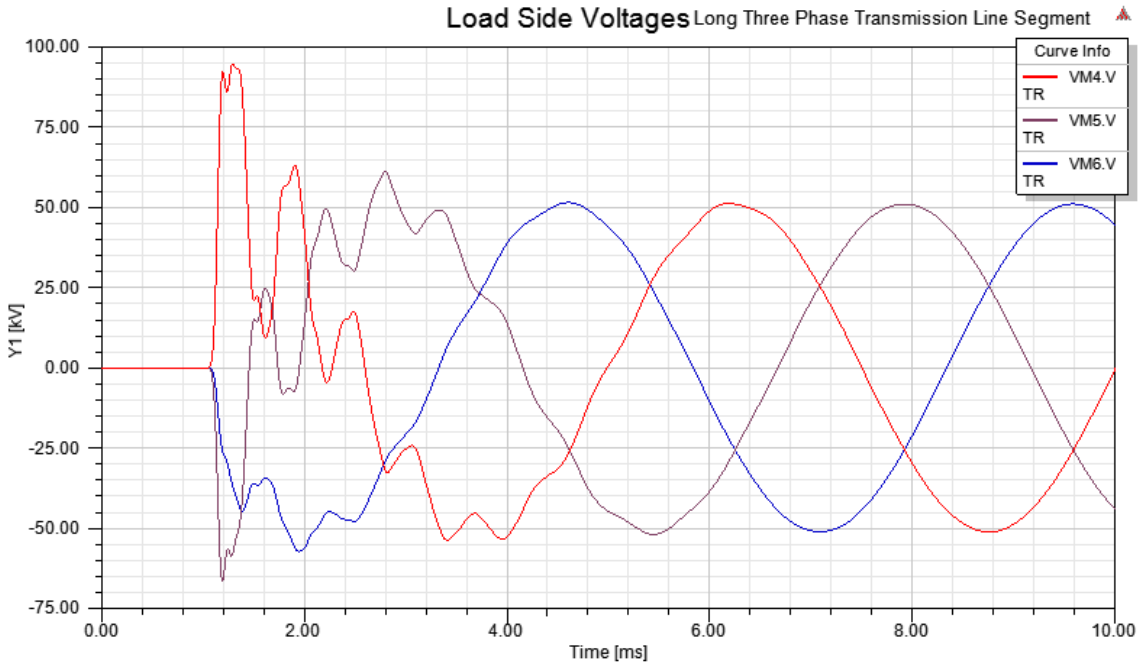


Figure 3: Load Voltages

The source/load voltages comparison is shown in Figure 4.

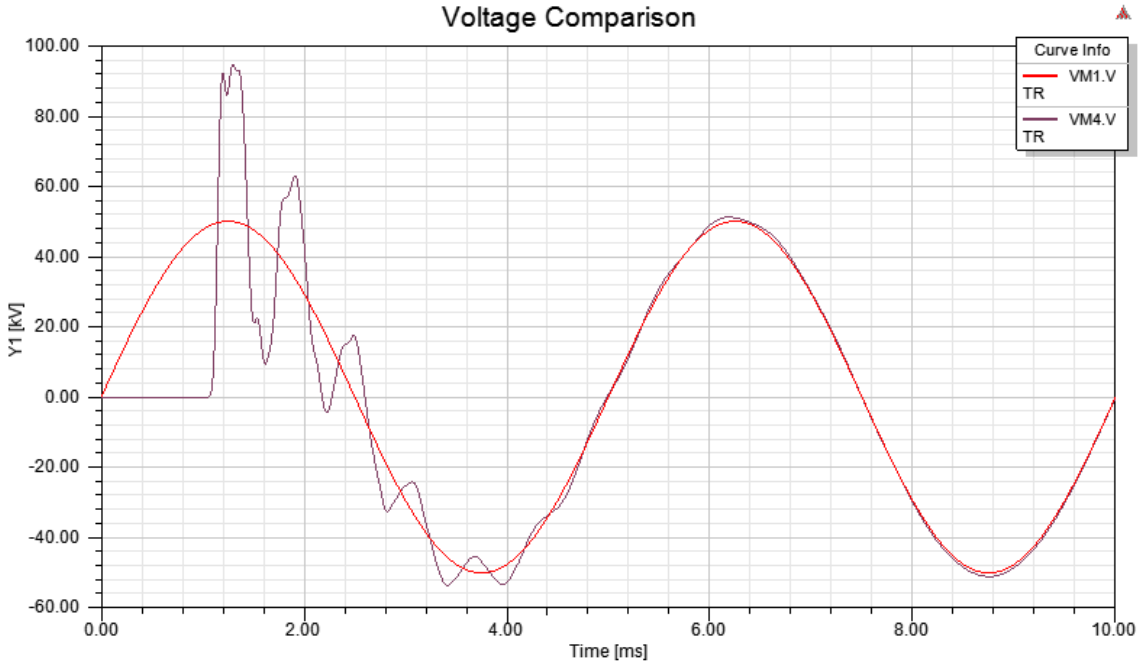


Figure 4: Source/Load Voltages Comparison

Transmission Line Medium Single Phase PI Example

Description

The transmission line medium single phasePIschematic is shown in Figure 1.

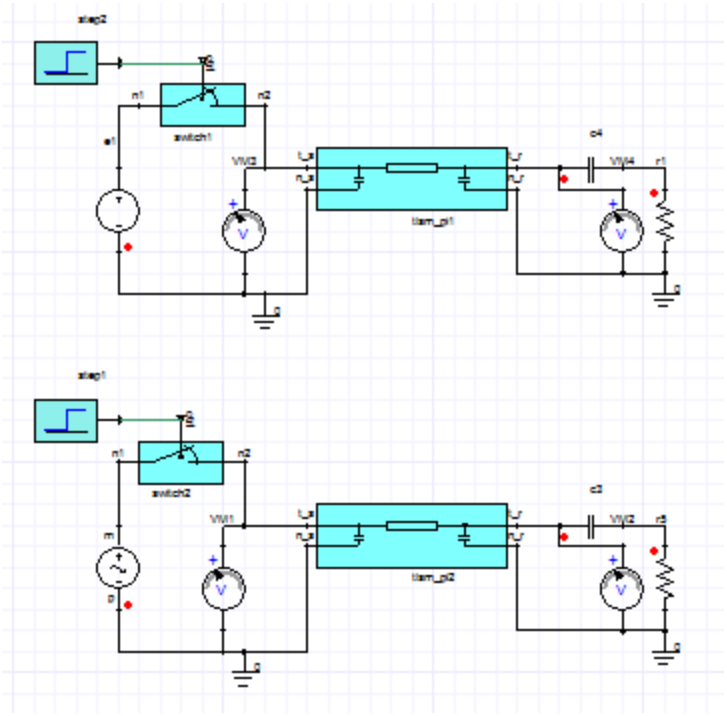


Figure 1: Transmission Line Medium Single Phase PISchematic

The system contains thetlsm_pi and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofsingle phase medium transmission line, nominal PI component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The DC voltages comparison is shown in Figure 2.

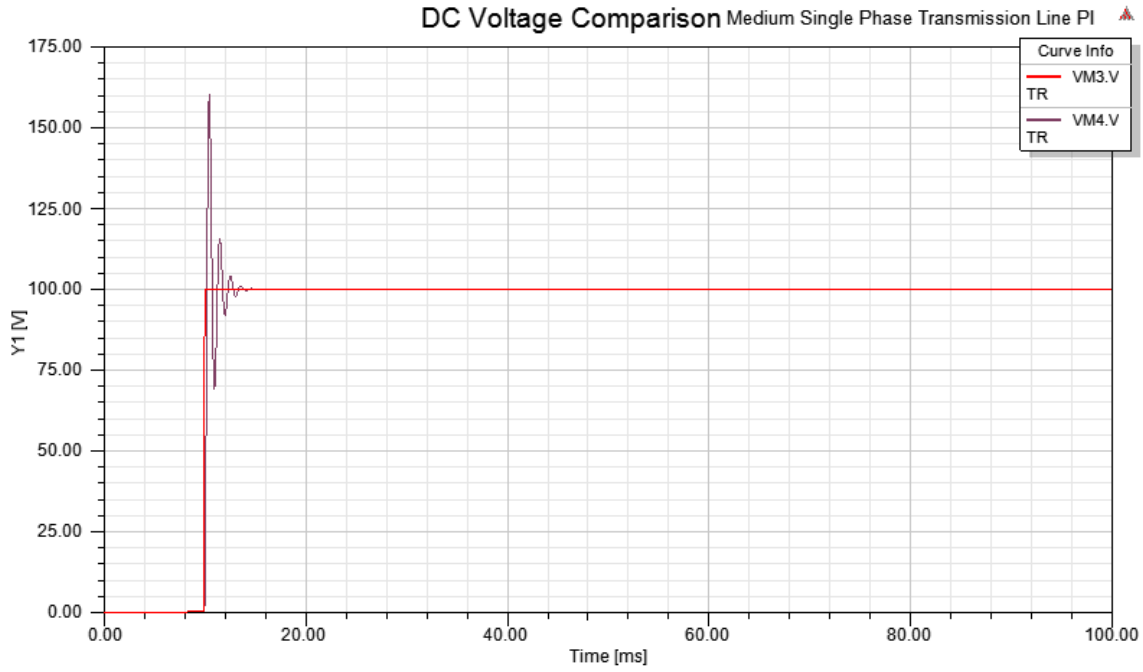


Figure 2: DC Voltage Comparison

The AC voltages comparison is shown in Figure 3.

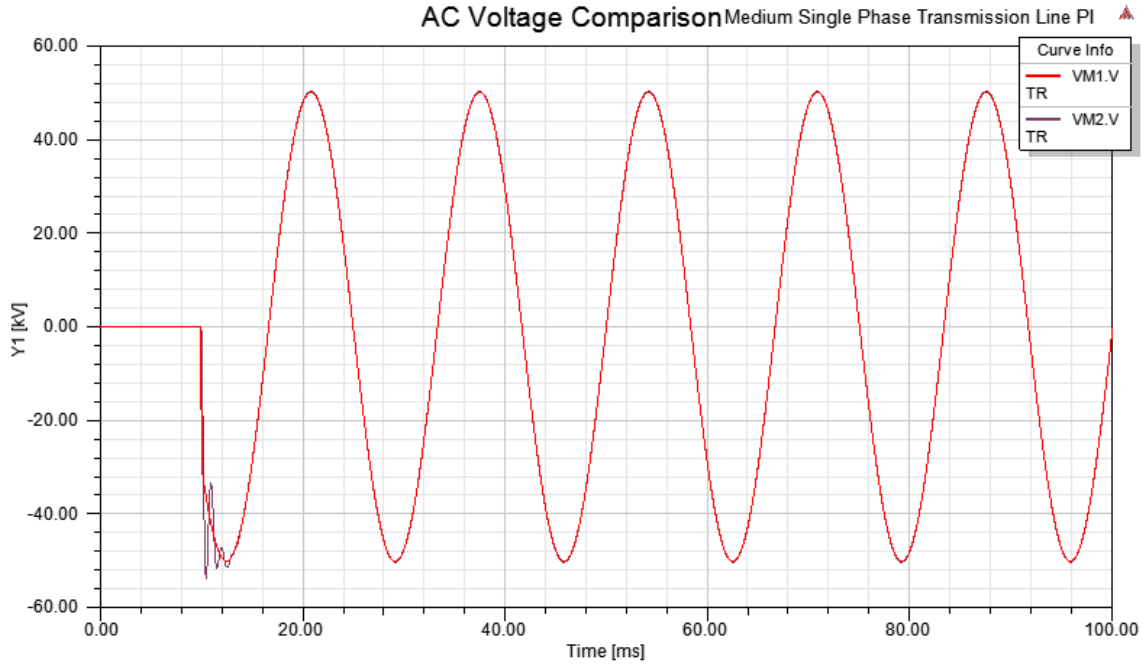


Figure 3: AC Voltage Comparison

Transmission Line Medium Single Phase T Example

Description

The transmission line medium single phaseTschematic is shown in Figure 1.

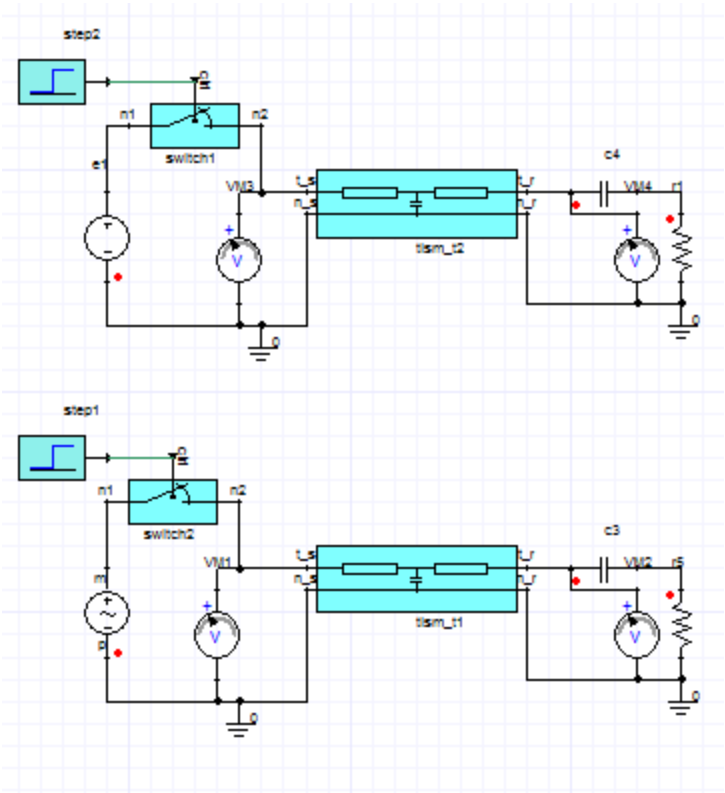


Figure 1: Transmission Line Medium Single Phase TSchematic

The system contains thetlsm_t and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofsingle phase medium transmission line, nominal T component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The DC voltages comparison is shown in Figure 2.

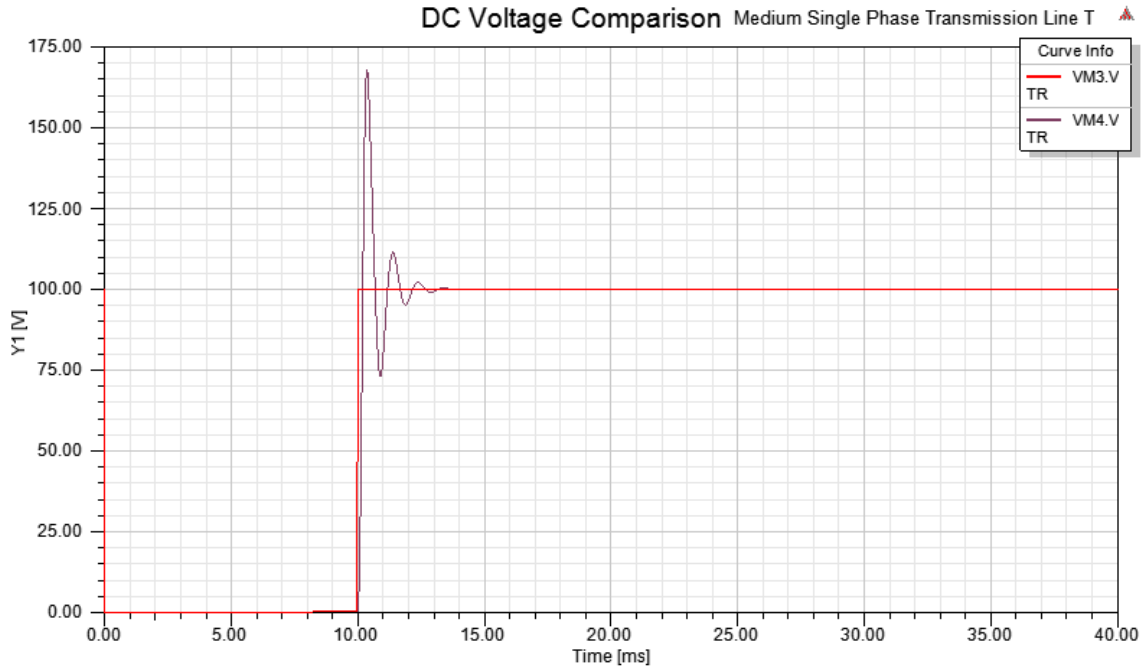


Figure 2: DC Voltage Comparison

The AC voltages comparison is shown in Figure 3.

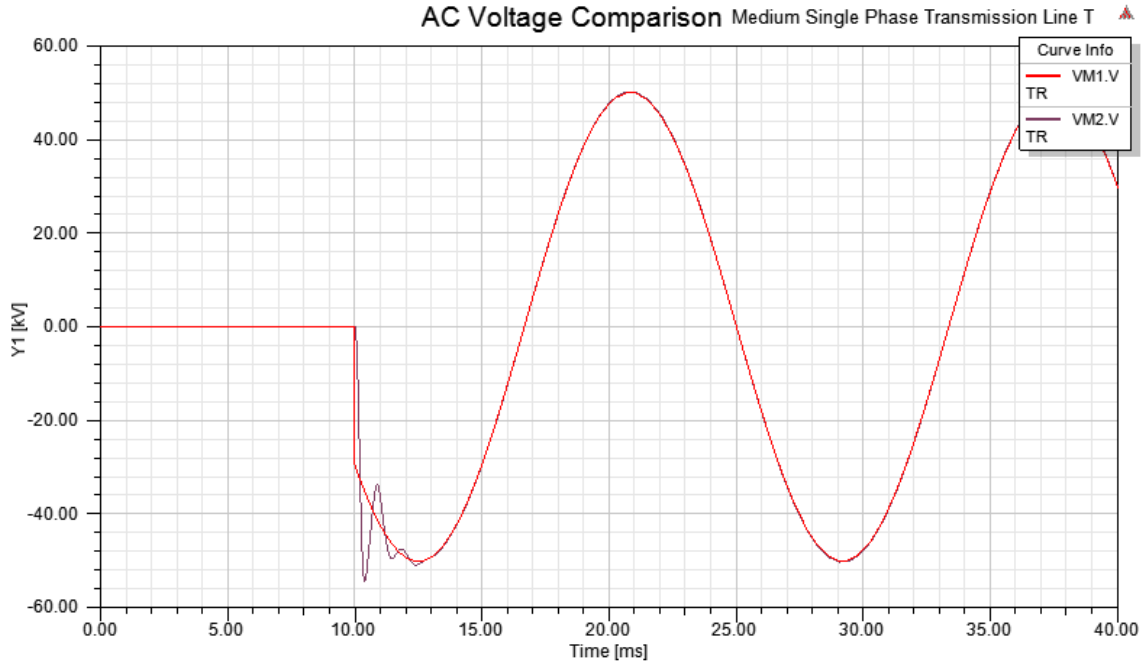


Figure 3: AC Voltage Comparison

Transmission Line Medium Three Phase PI Example

Description

The transmission line medium three phase PI schematic is shown in Figure 1.

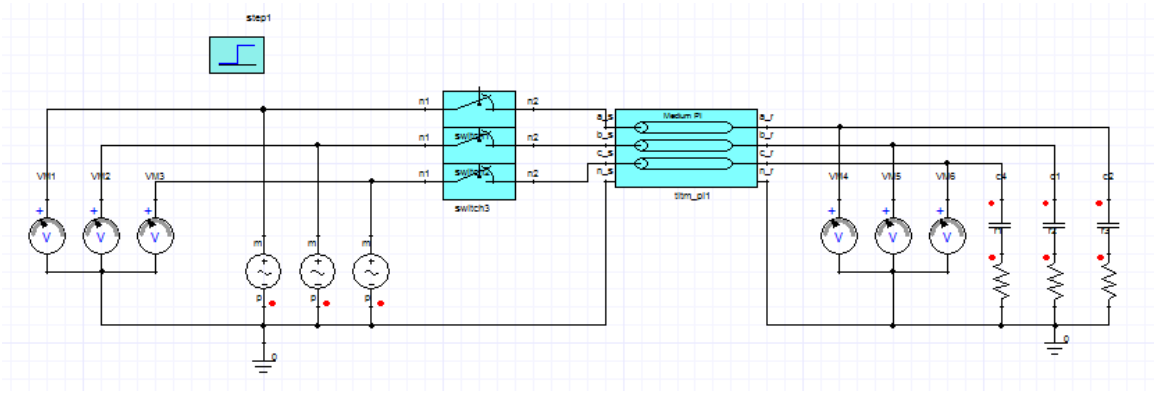


Figure 1: Transmission Line Medium Three Phase PISchematic

The system contains thetltm_pi and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofthree phase medium transmission line, nominal PI component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The source voltages are shown in Figure 2.

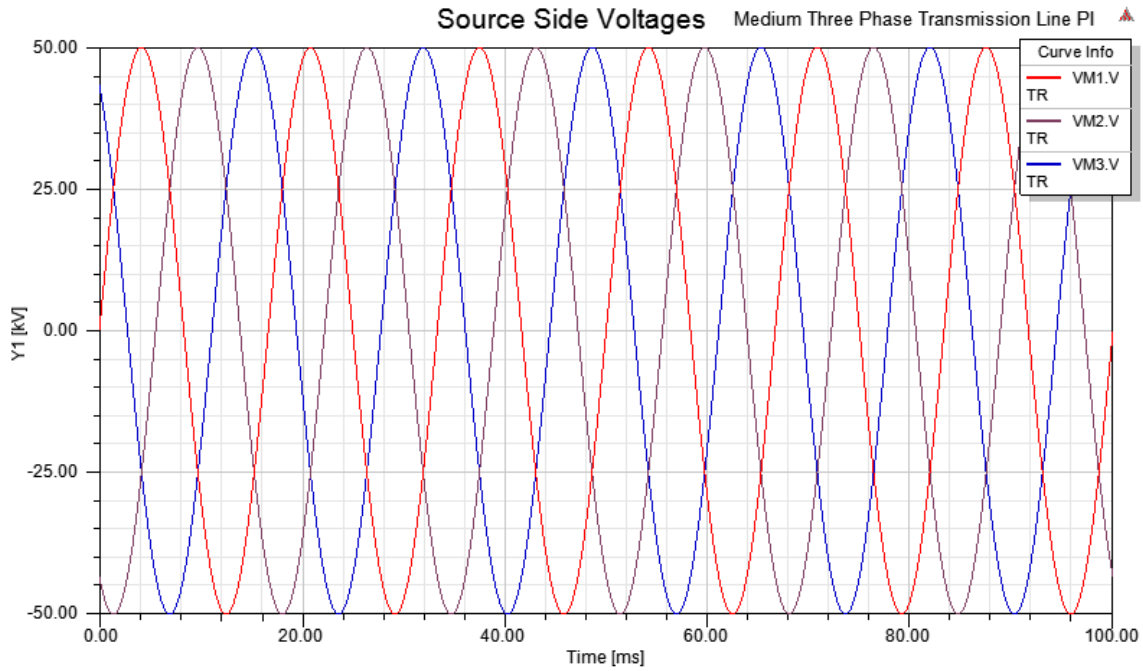


Figure 2: Source Voltages

The load voltages are shown in Figure 3.

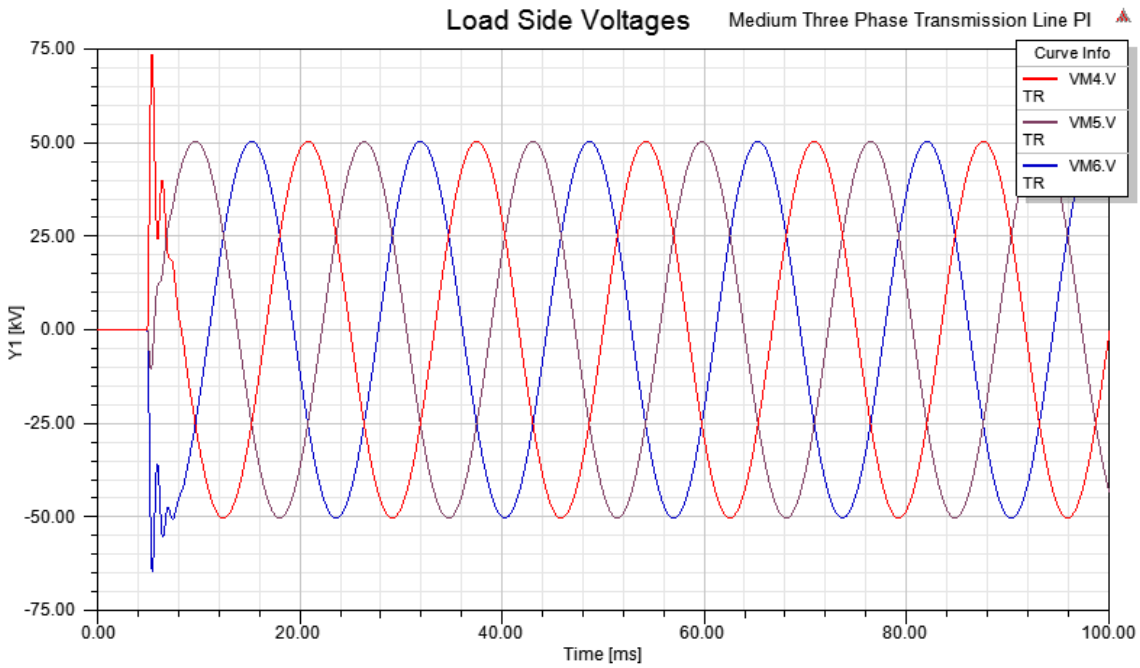


Figure 3: Load Voltages

The source/load voltages comparison is shown in Figure 4.

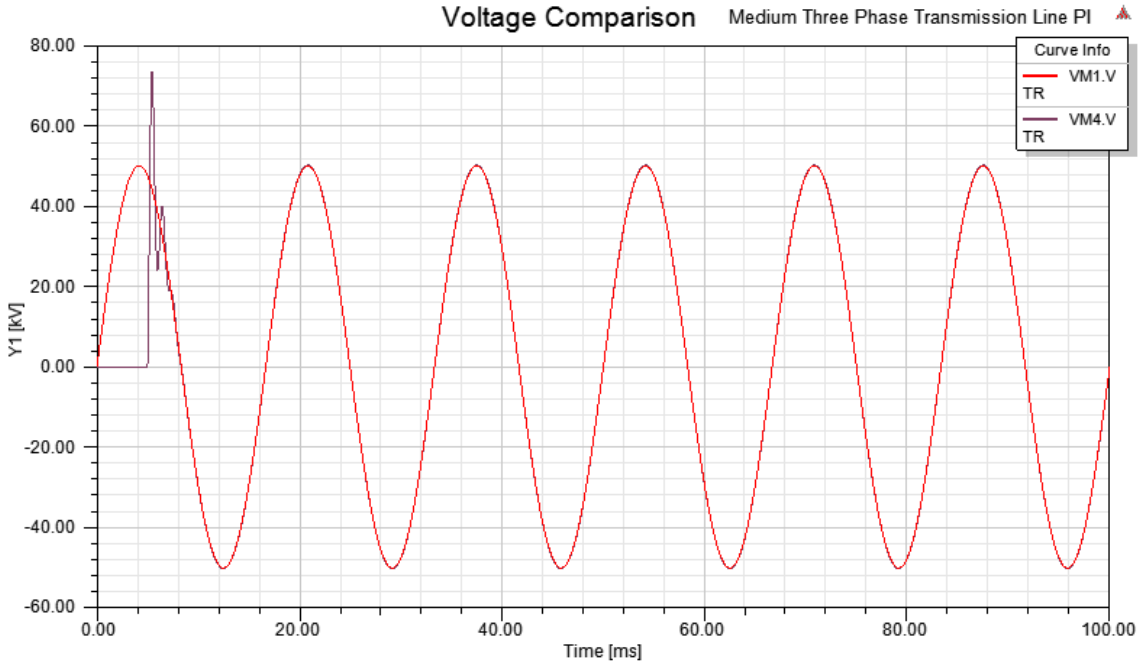


Figure 4: Source/Load Voltages Comparison

Transmission Line Medium Three Phase T Example

Description

The transmission line medium three phase T schematic is shown in Figure 1.

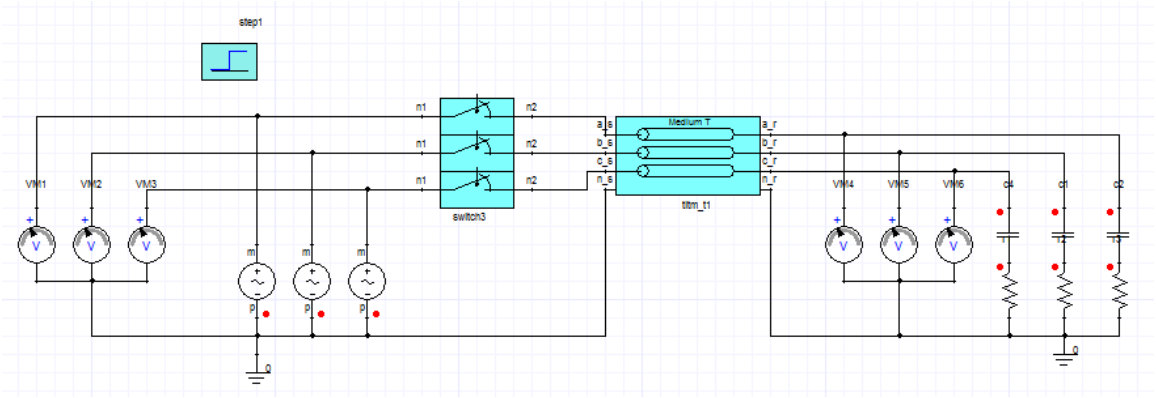


Figure 1: Transmission Line Medium Three Phase TSchematic

The system contains thetltm_t and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofthree phase medium transmission line, nominal T component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The source voltages are shown in Figure 2.

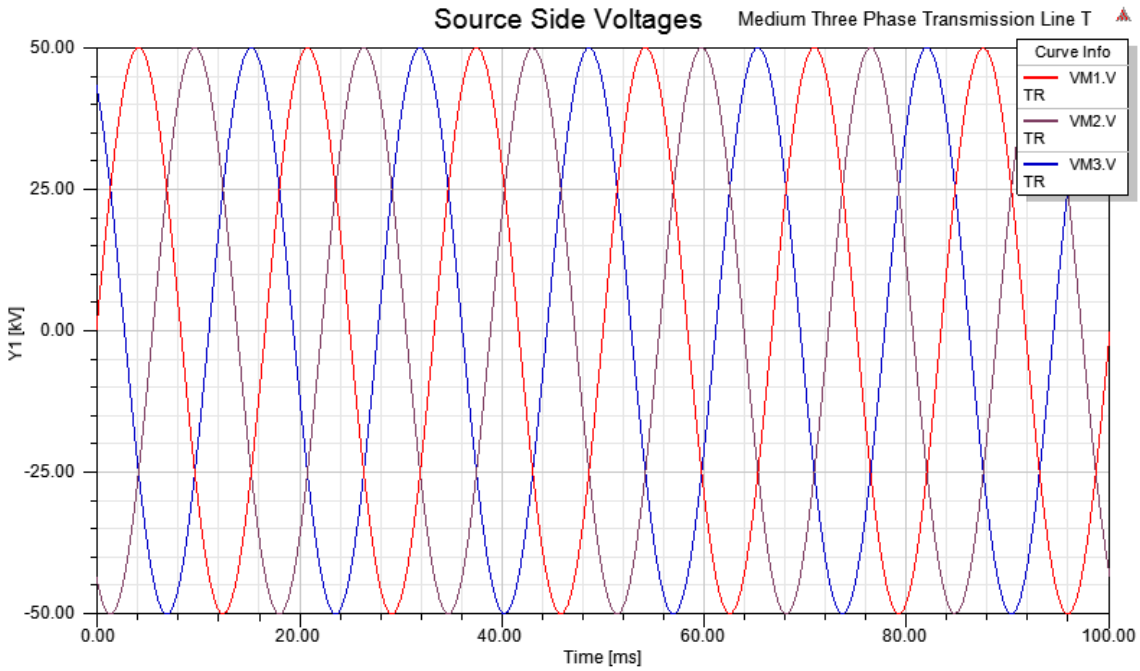


Figure 2: Source Voltages

The load voltages are shown in Figure 3.

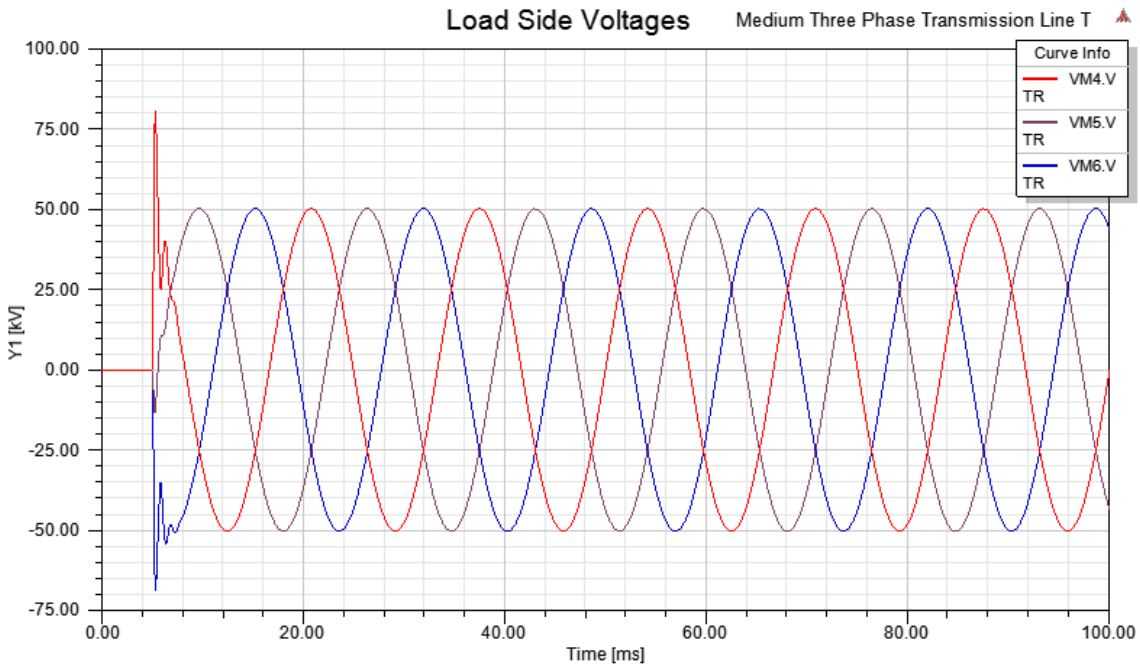


Figure 3: Load Voltages

The source/load voltages comparison is shown in Figure 4.

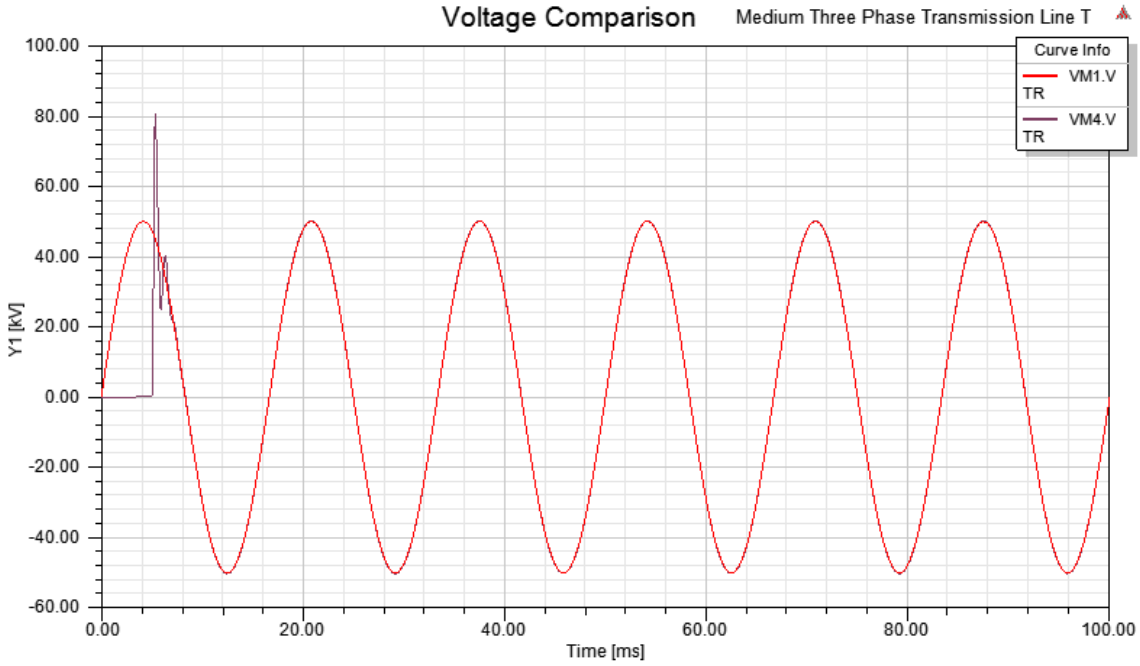


Figure 4: Source/Load Voltages Comparison

Transmission Line Short Single Phase Example

Description

The transmission line short single phase schematic is shown in Figure 1.

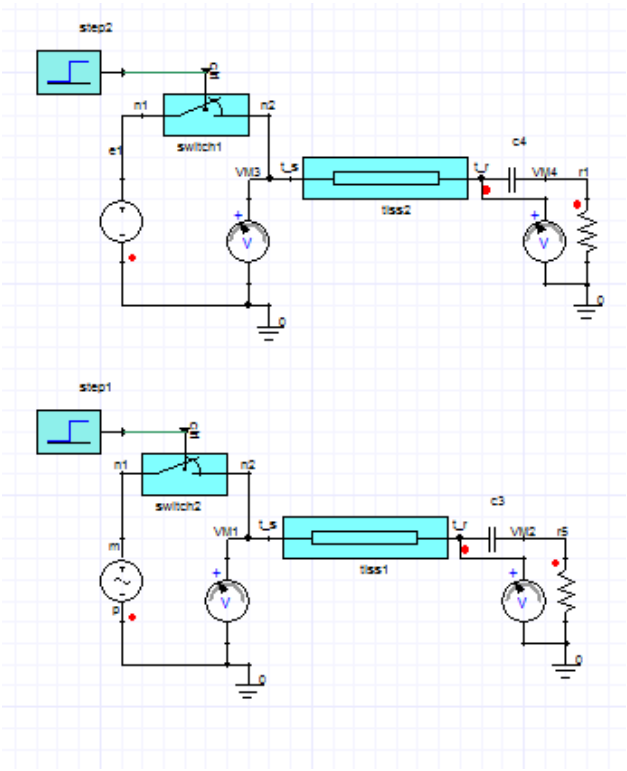


Figure 1: Transmission Line Short Single PhaseSchematic

The system contains thetlss and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofsingle phase short transmission line component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The DC voltages comparison is shown in Figure 2.

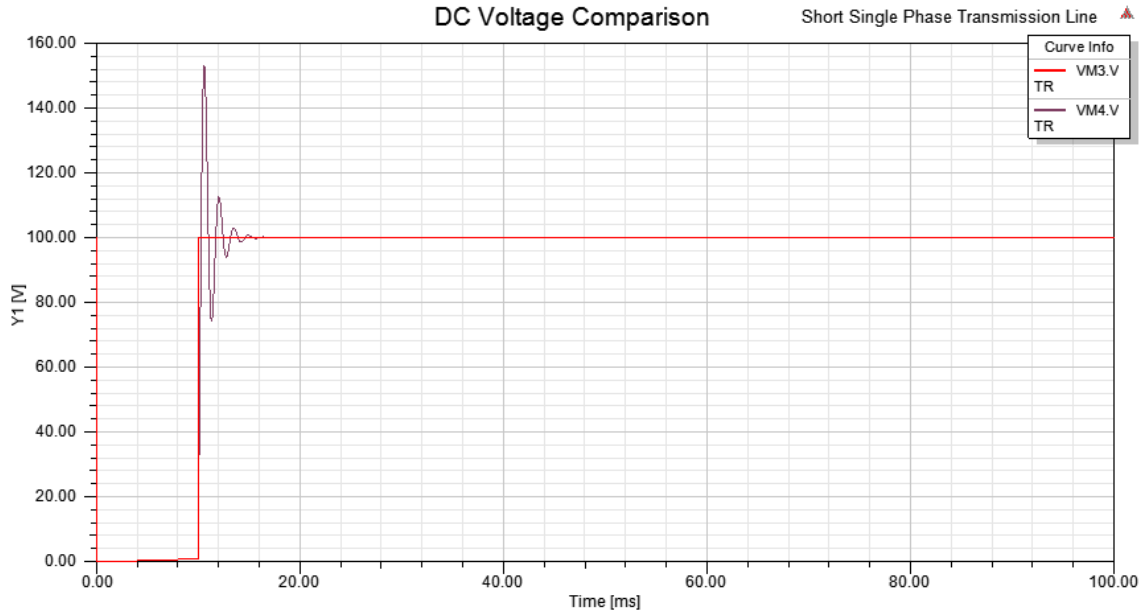


Figure 2: DC Voltage Comparison

The AC voltages comparison is shown in Figure 3.

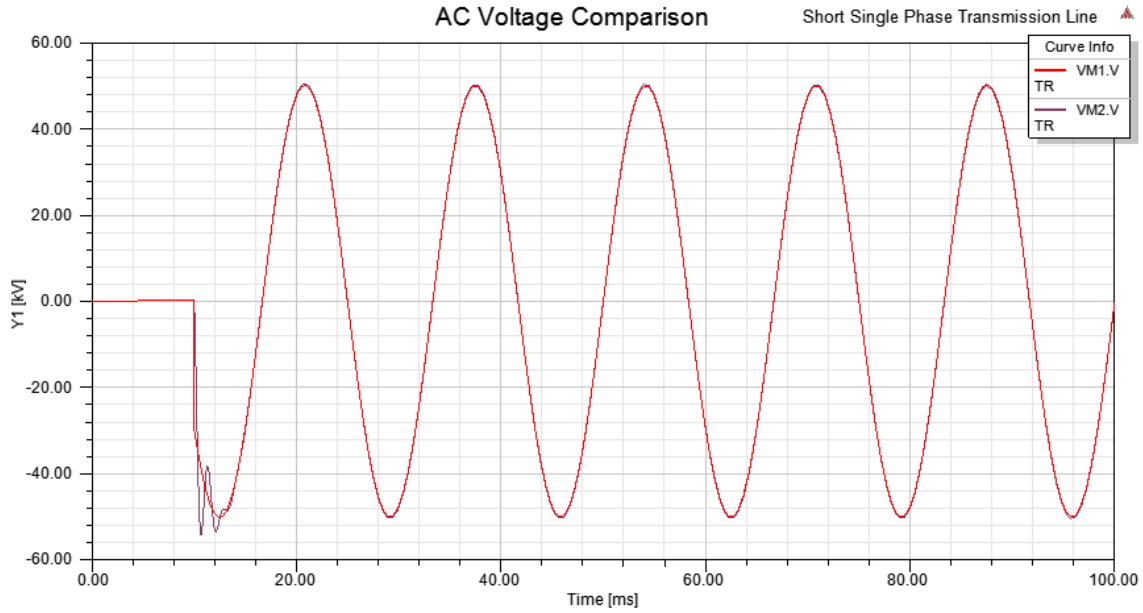


Figure 3: AC Voltage Comparison

Transmission Line Short Three Phase Example

Description

The transmission line short three phase schematic is shown in Figure 1.

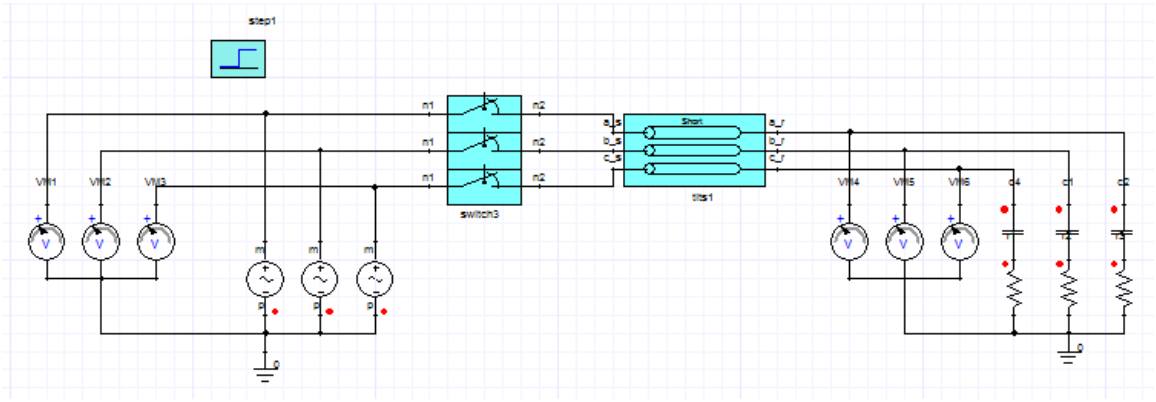


Figure 1: Transmission Line Short Three PhaseSchematic

The system contains thetlts and switchmodels from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage ofthree phase short transmission line component in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The source voltages are shown in Figure 2.

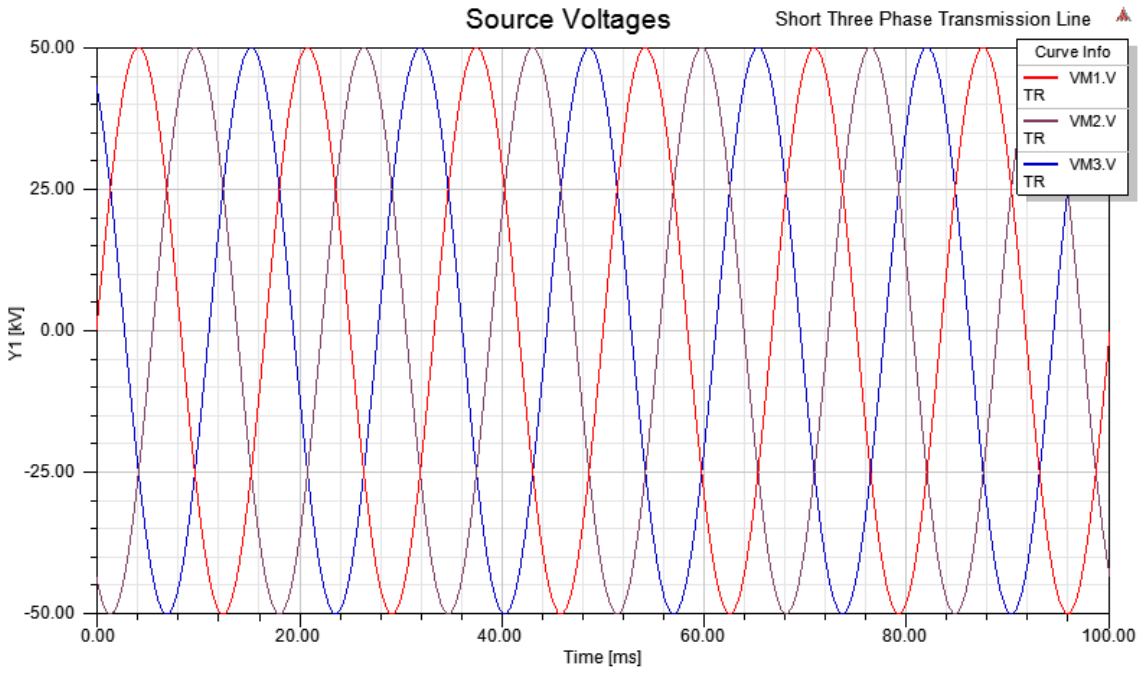


Figure 2: Source Voltages

The load voltages are shown in Figure 3.

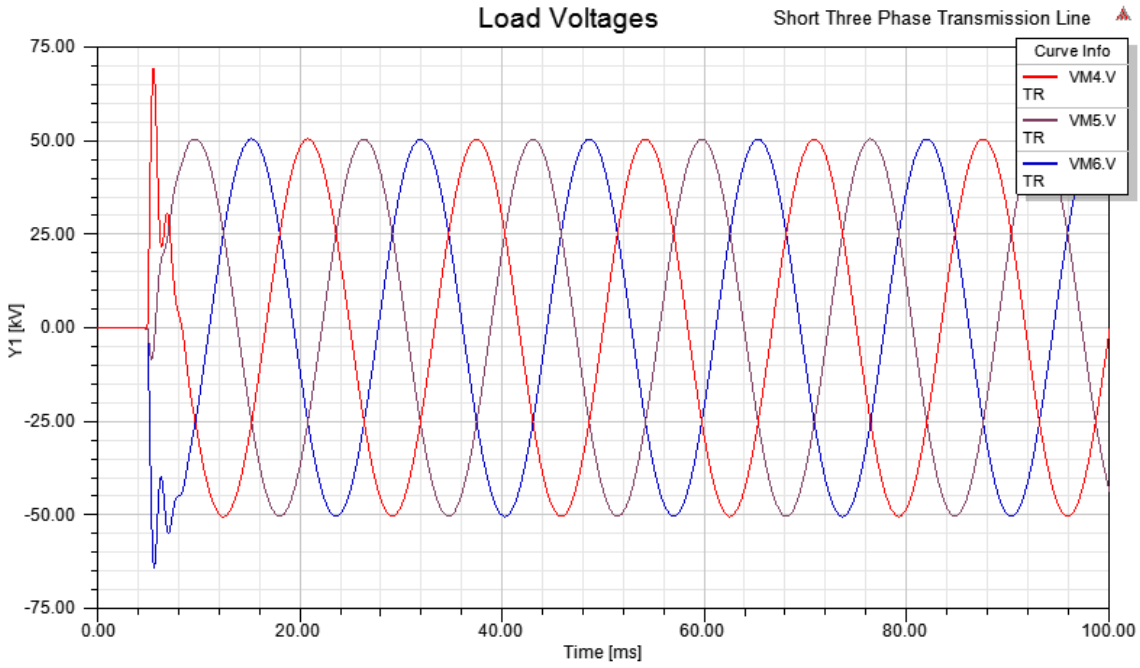


Figure 3: Load Voltages

The source/load voltages comparison is shown in Figure 4.

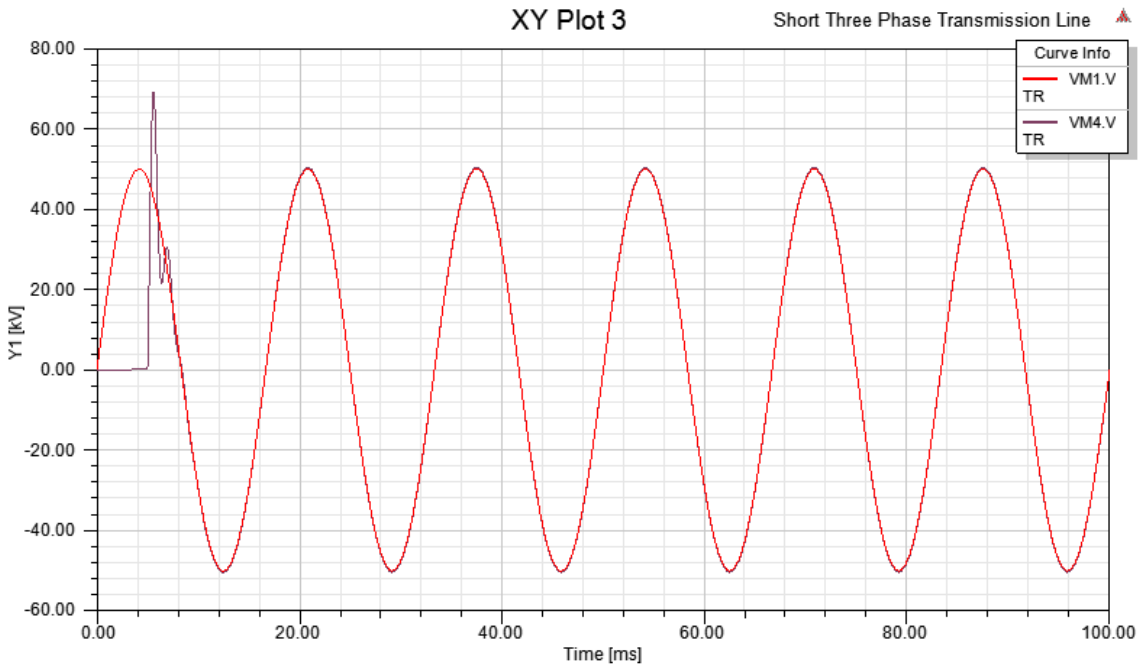


Figure 4: Source/Load Voltages Comparison

Transformations Example

Description

The transformations schematic is shown in Figure 1.

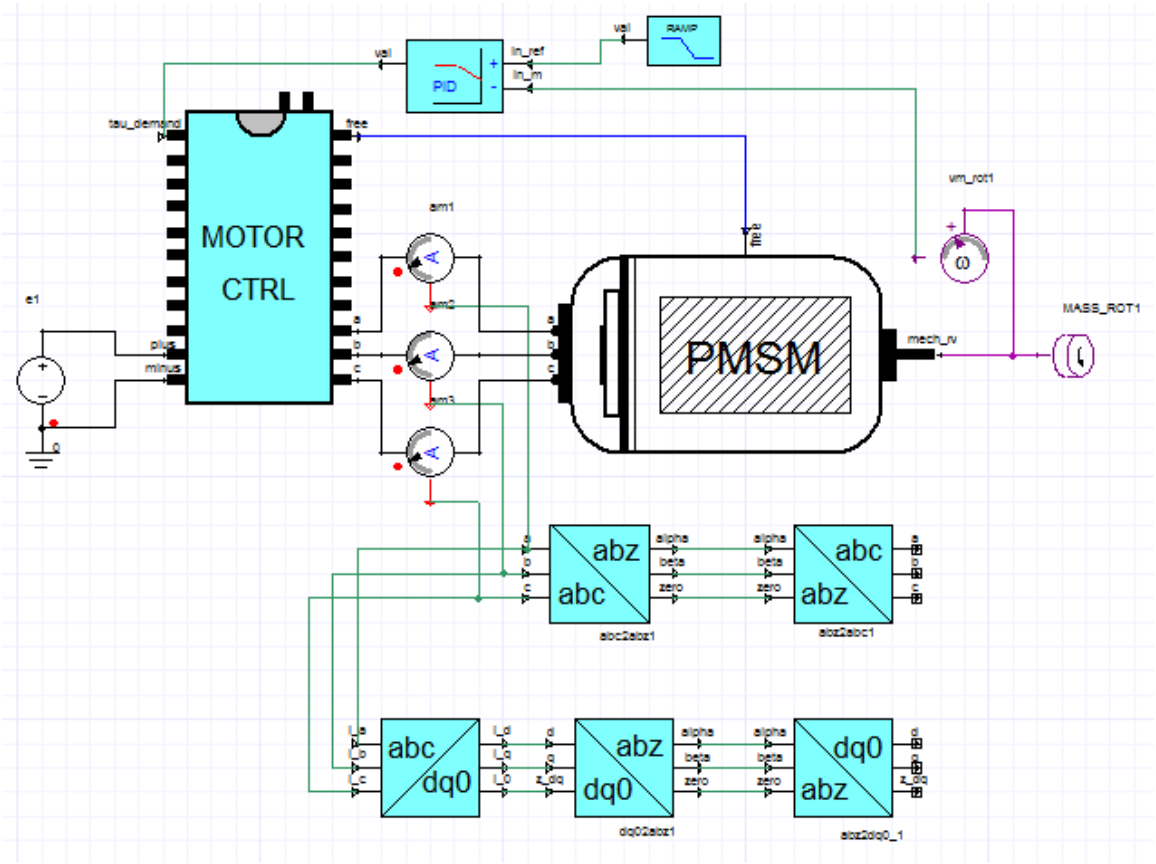


Figure 1: TransformationsSchematic

The system contains the c_motor_dcac, pid_lim, motor_pm, ramp and abc2dq0 models from the Aircraft Electrical VHDL-AMS library, abc2abz, abz2abc, dq02abz and abz2dq0 models from the Power System VHDL-AMSlibrary.

This example is mainly used for demonstrating the usage of transformation between abc, alpha-beta-zero and dq0. The results from the transmission components are shown.

Simulation Results

The signals of abc to alpha-beta-zero transformation are shown in Figure 2.

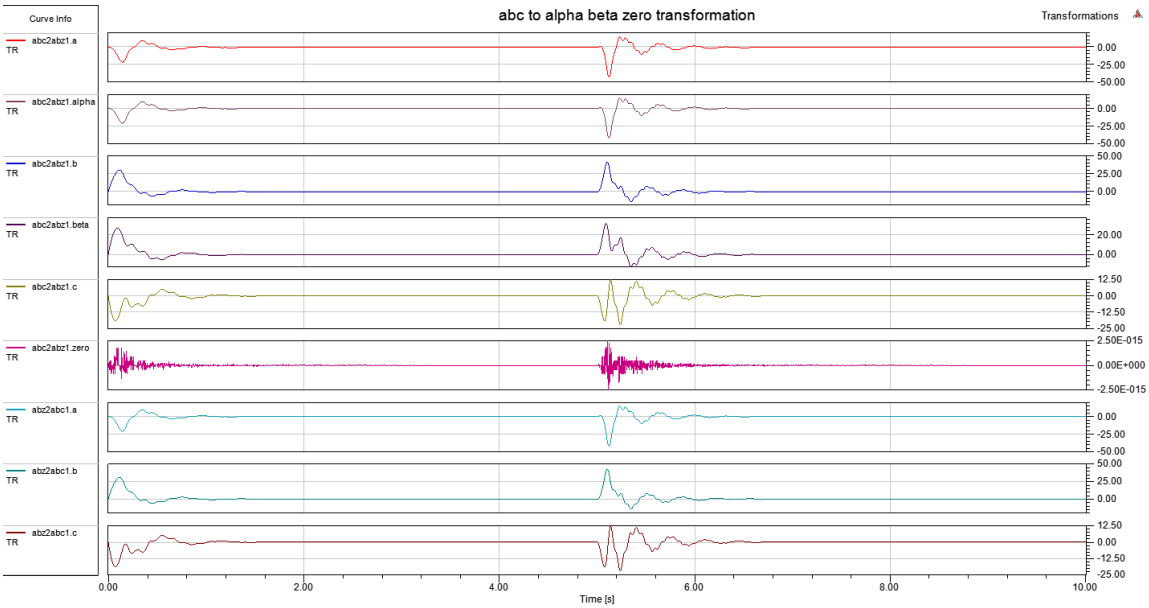


Figure 2: abc to alpha-beta-zero Transformation

The signals of dq0 to alpha-beta-zero transformation are shown in Figure 3.

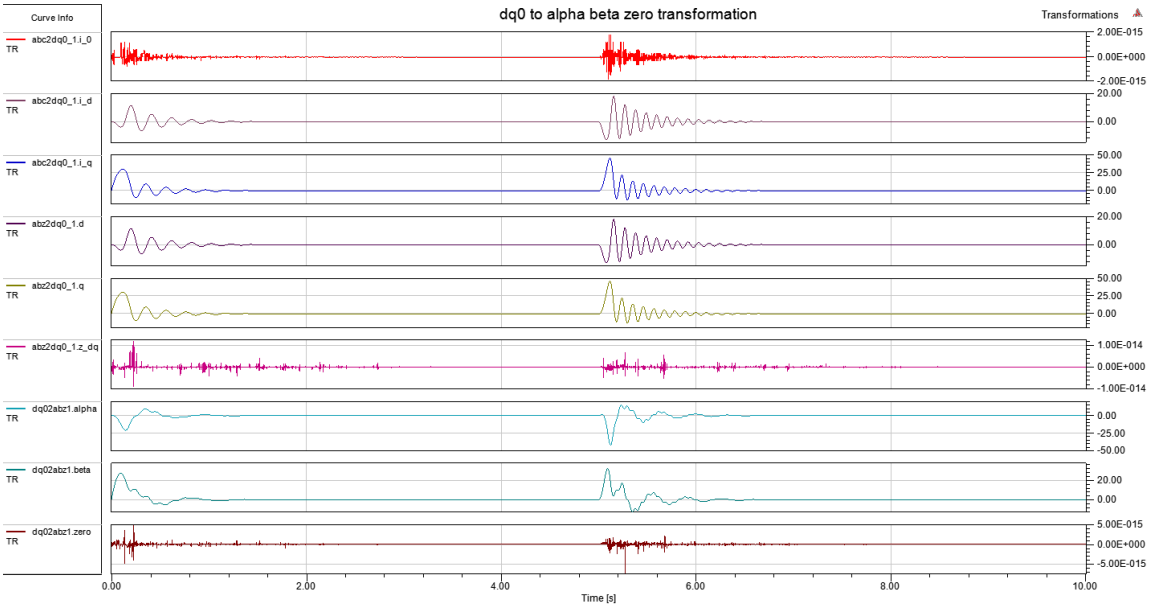


Figure 3: dq0 to alpha-beta-zero Transformation

Transformer Delta-Delta Connection Example

Description

The transformer Delta-Delta connection schematic is shown in Figure 1.

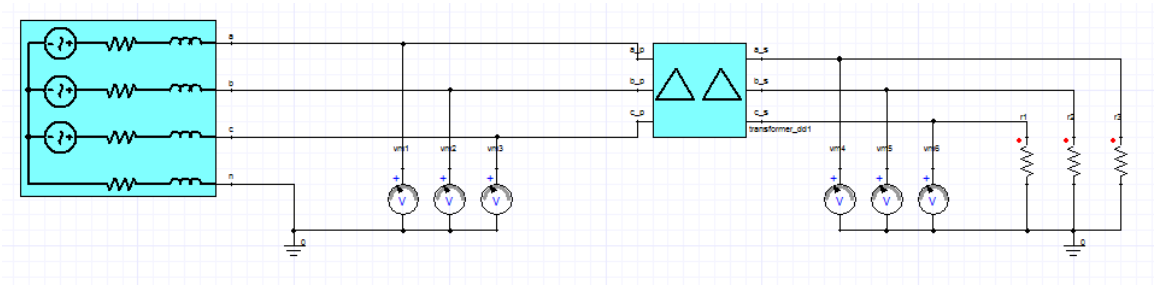


Figure 1: Transformer Delta-Delta Connection Example Schematic

The system contains the transformer_dd from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer delta-delta connection in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

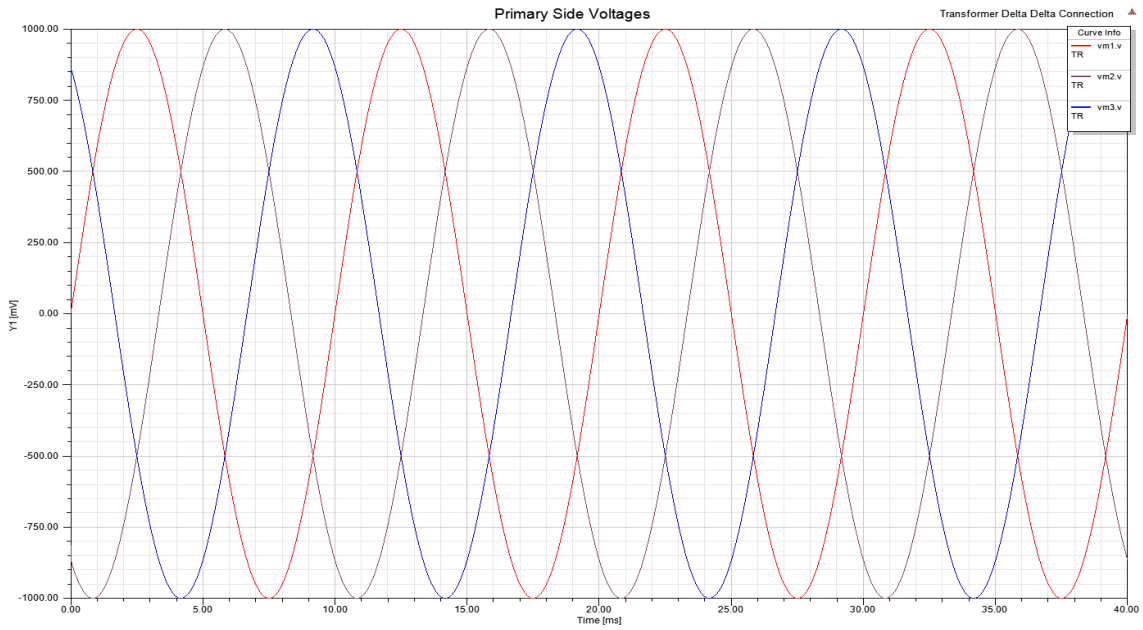


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

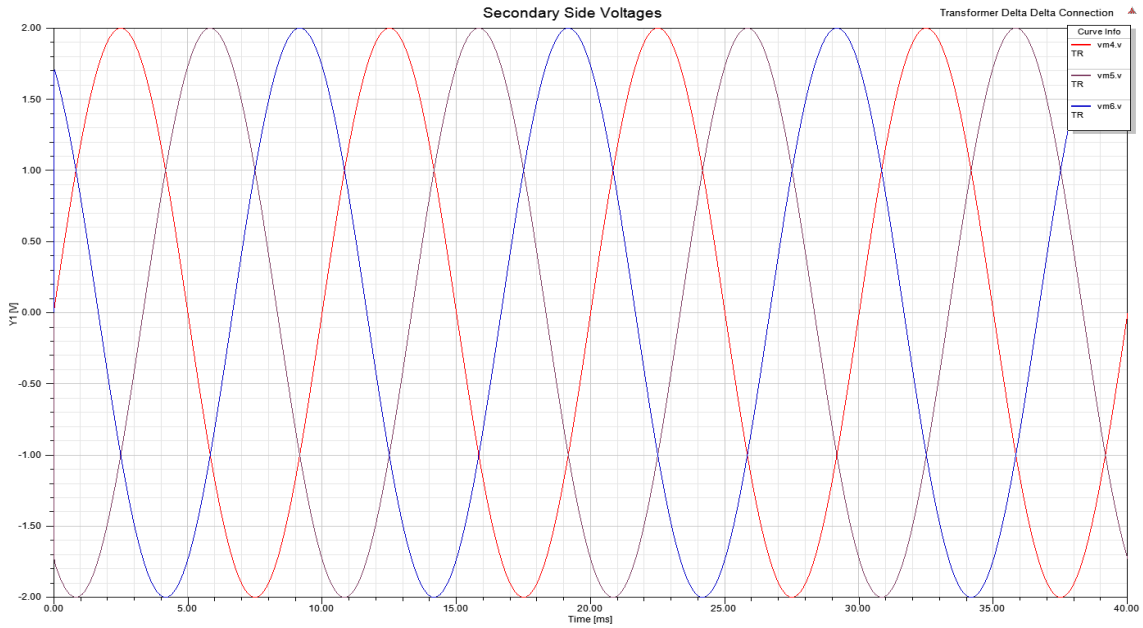


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

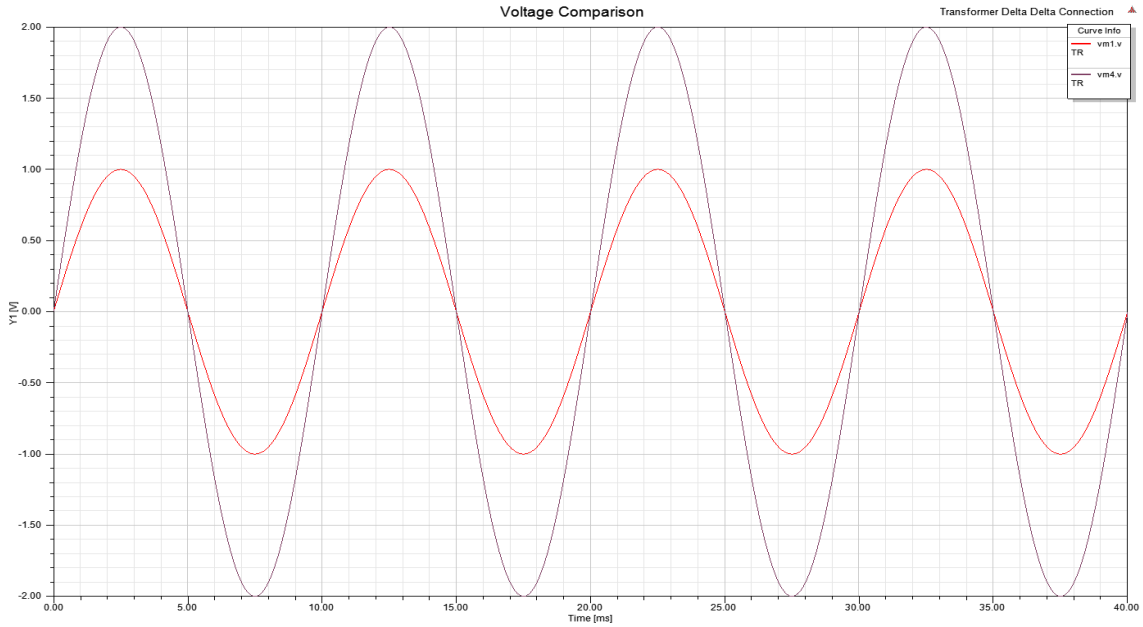


Figure 4: Voltage Comparison

Transformer Delta-Delta-Wye Connection Lag Example

Description

The transformer Delta-Delta-Wye connectionlagschematic is shown in Figure 1.

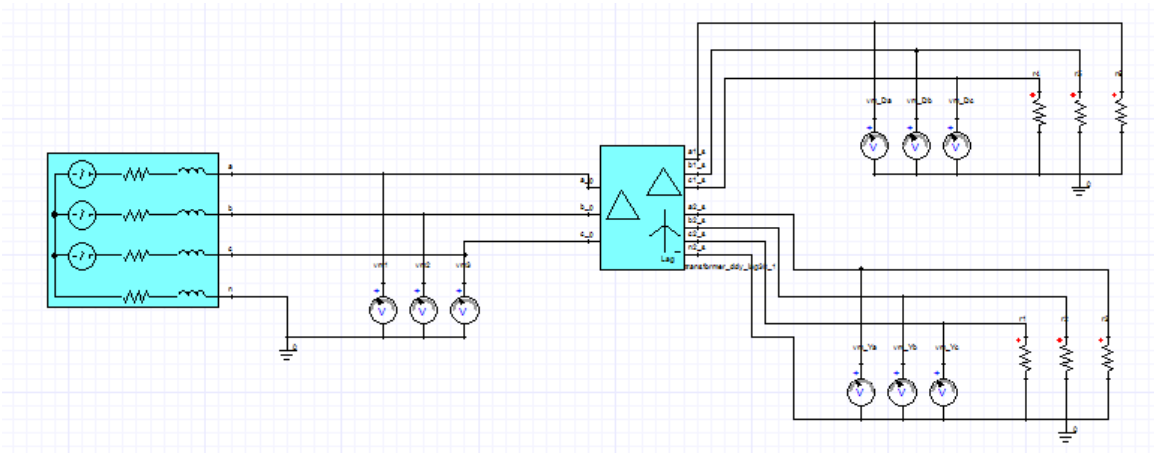


Figure 1: Transformer Delta-Delta-Wye Connection Lag Example Schematic

The system contains the transformer_ddy_lag from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer delta-delta-wye connection lag in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

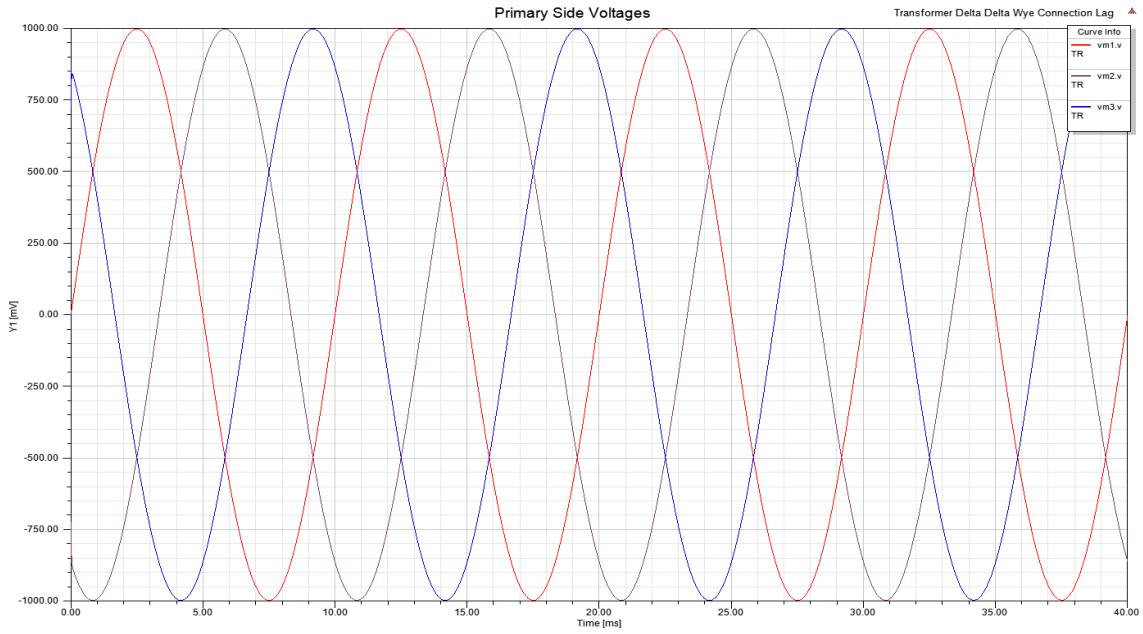


Figure 2: Primary Side Voltages

The secondary side Delta connection voltages are shown in Figure 3.

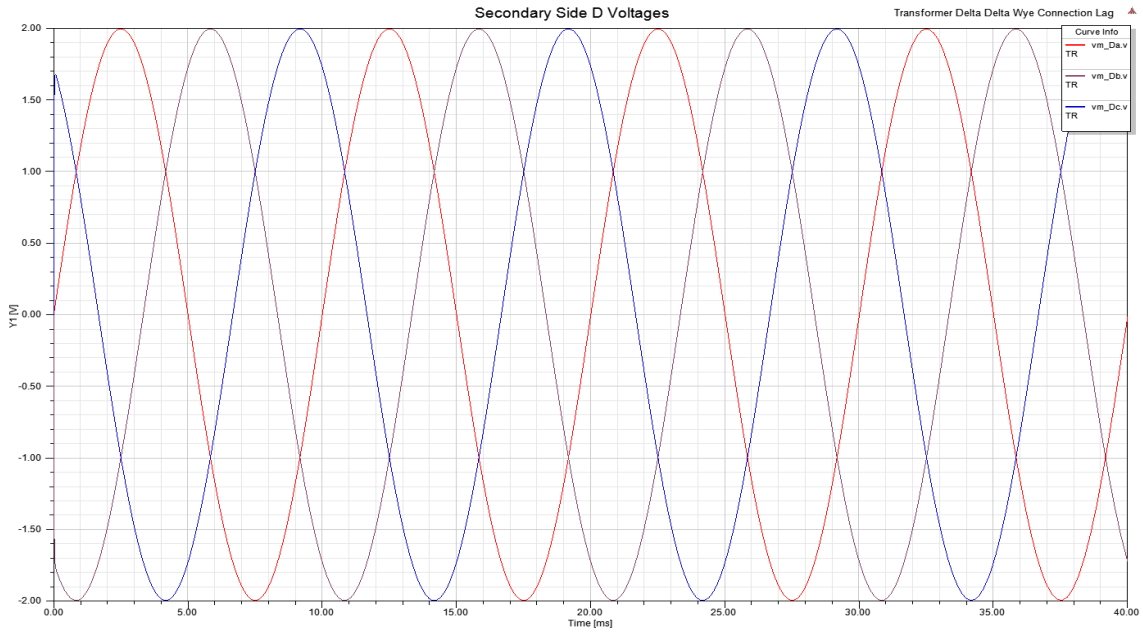


Figure 3: Secondary Side D Voltages

The secondary side Wye connection voltages are shown in Figure 4.

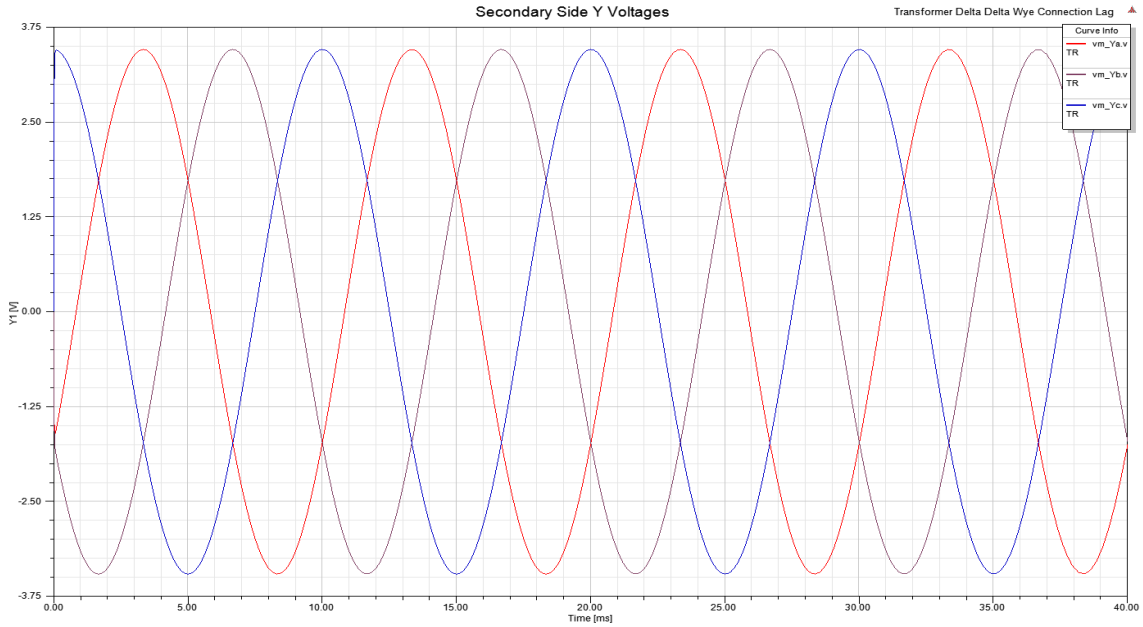


Figure 4: Secondary Side Y Voltages

The voltage comparison are shown in Figure 5.

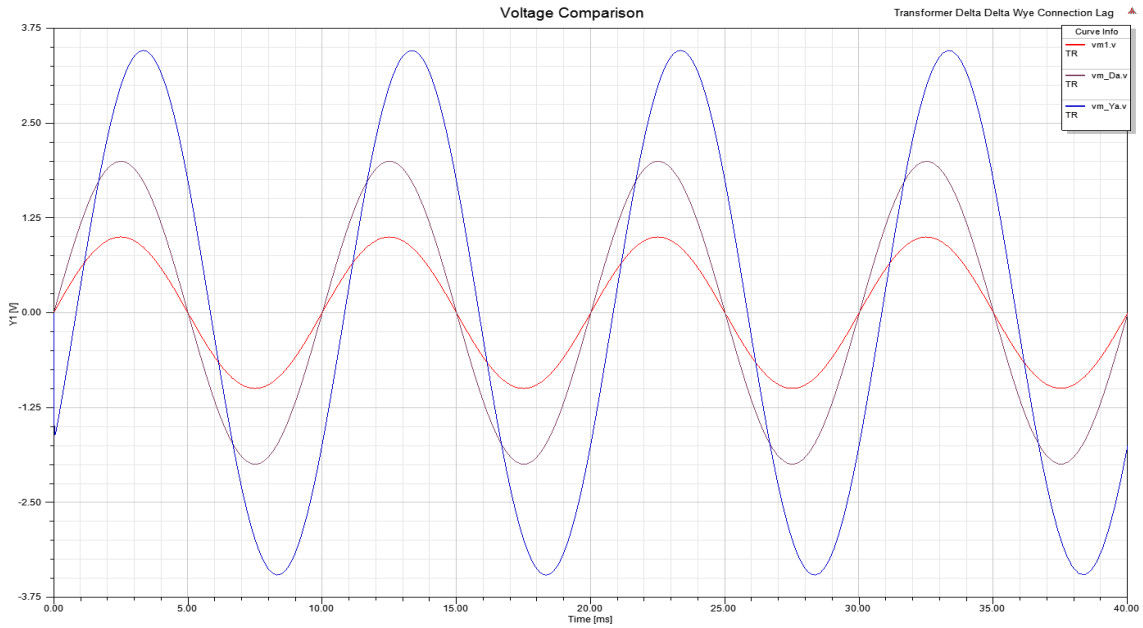


Figure 5: Voltage Comparison

Transformer Delta-Delta-Wye Connection Lead Example

Description

The transformer Delta-Delta-Wye connection lead schematic is shown in Figure 1.

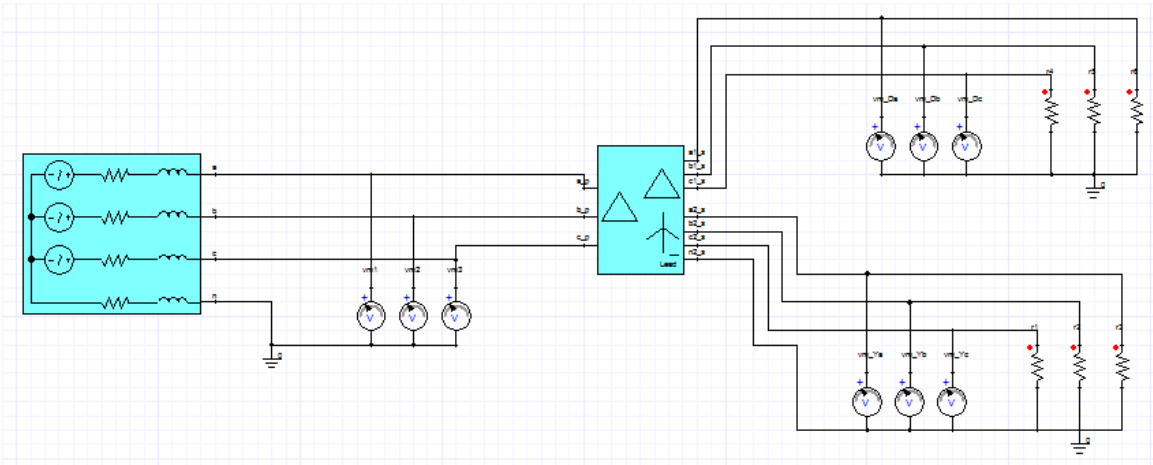


Figure 1: Transformer Delta-Delta-Wye Connection Lead Example Schematic

The system contains the transformer_ddy_lead30 from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer delta-delta-wye connection lead in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

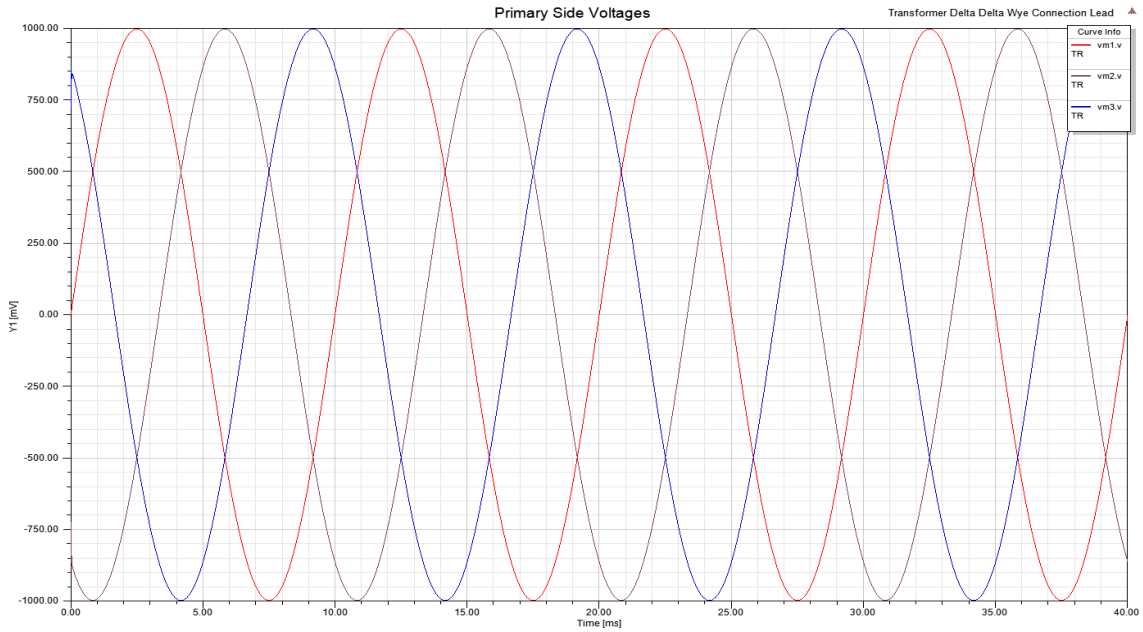


Figure 2: Primary Side Voltages

The secondary side Delta connection voltages are shown in Figure 3.

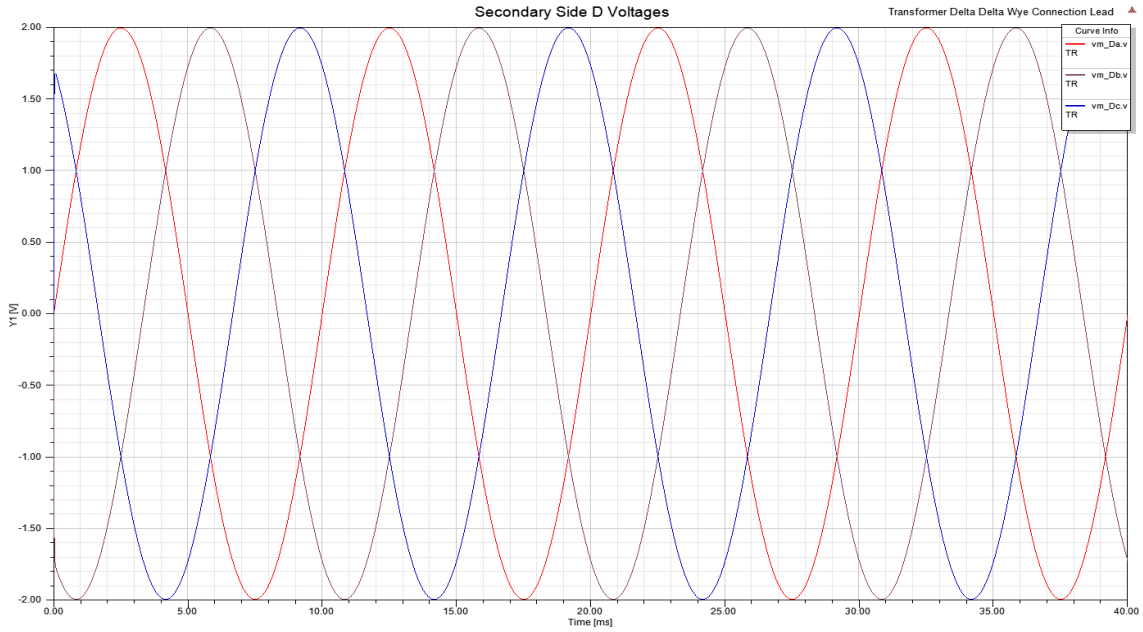


Figure 3: Secondary Side D Voltages

The secondary side Wye connection voltages are shown in Figure 4.

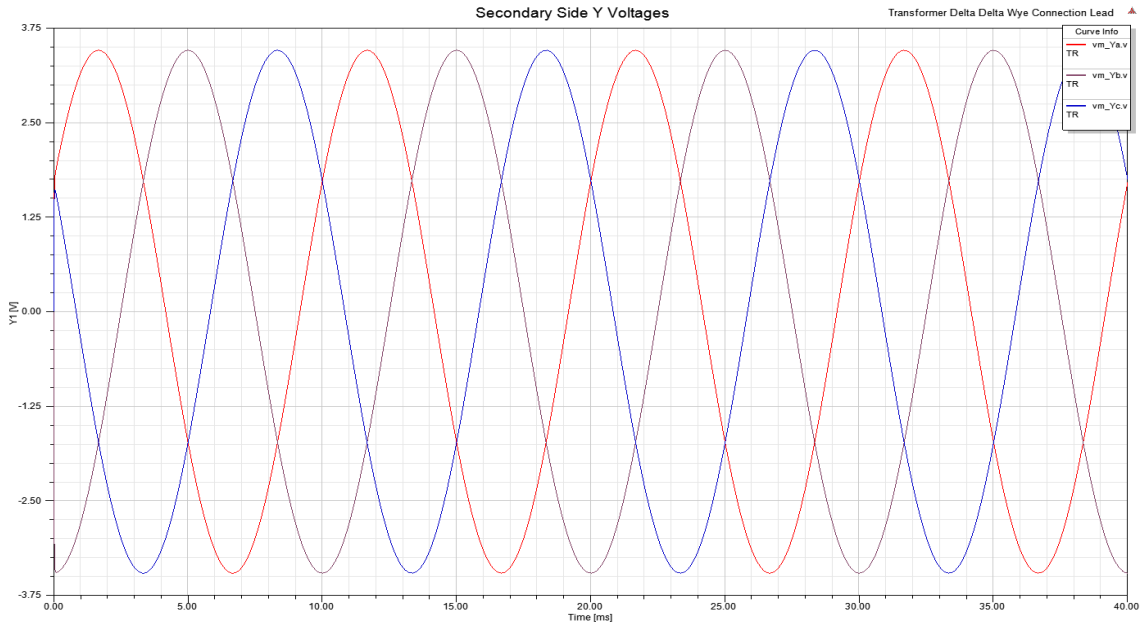


Figure 4: Secondary Side Y Voltages

The voltage comparison are shown in Figure 5.

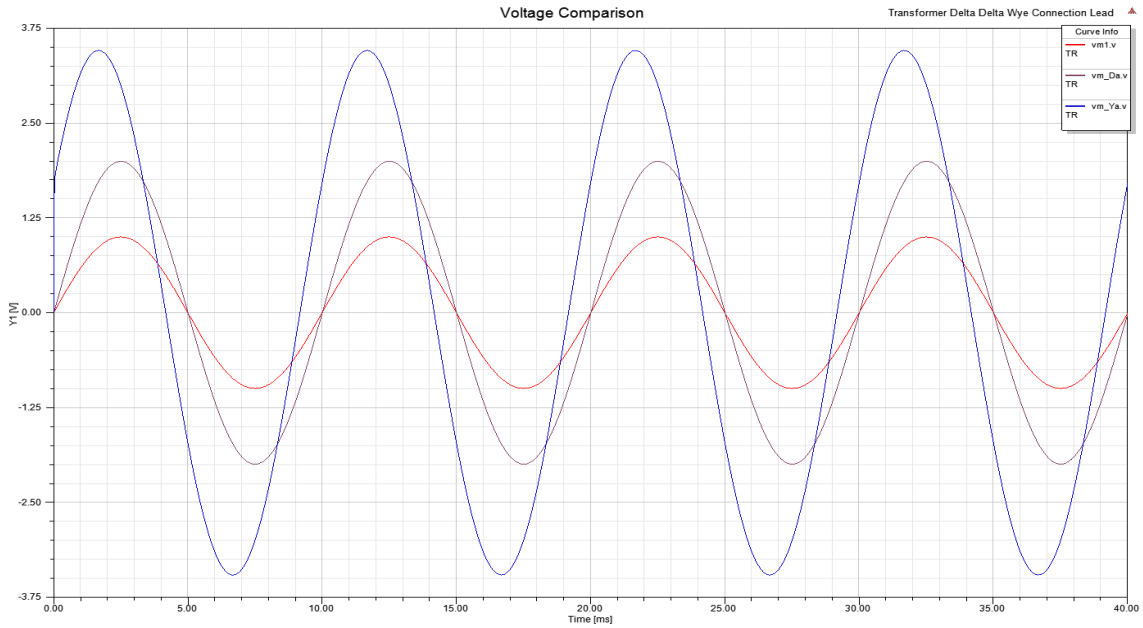


Figure 5: Voltage Comparison

Transformer Delta-Wye Connection Lag Example

Description

The transformer Delta-Wye connection lag schematic is shown in Figure 1.

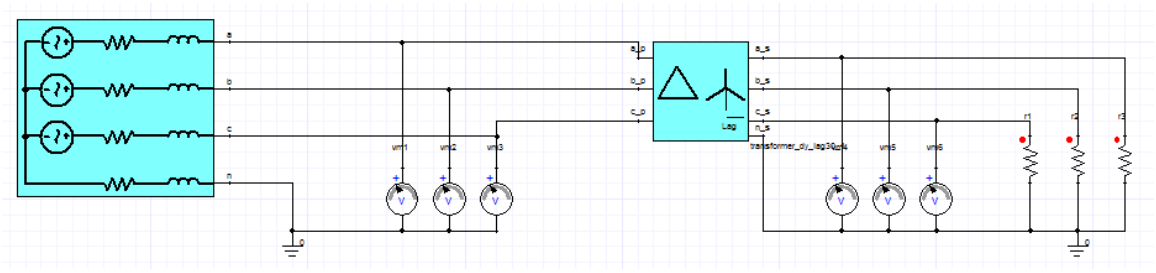


Figure 1: Transformer Delta-Wye Connection Lag Example Schematic

The system contains the transformer_dy_lag30 from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer delta-wye connection lag 30 degree in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

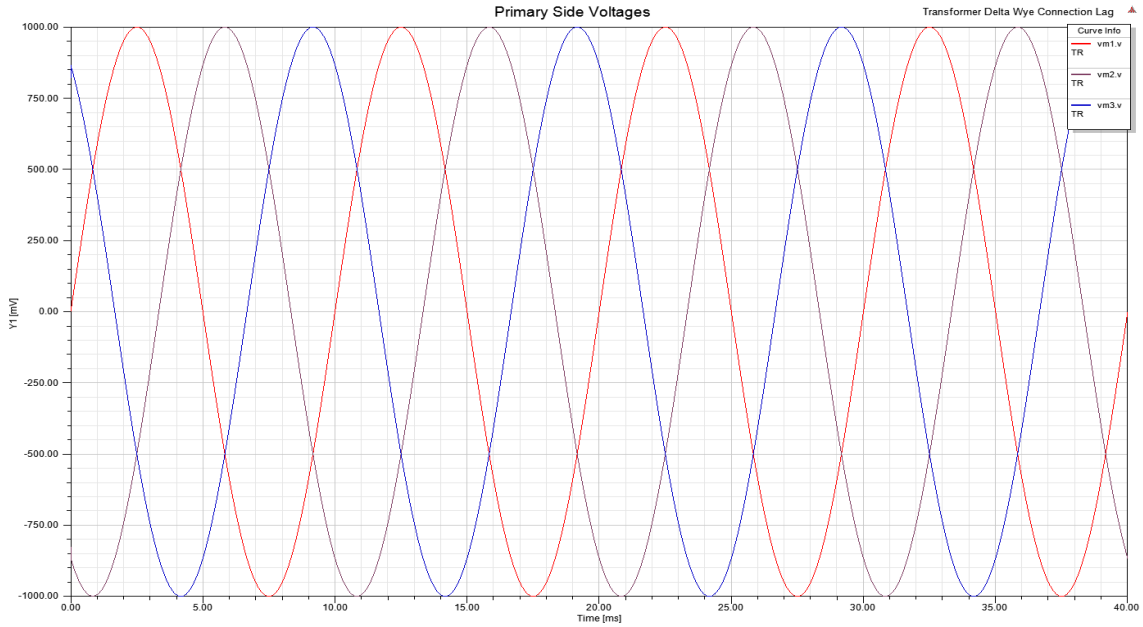


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

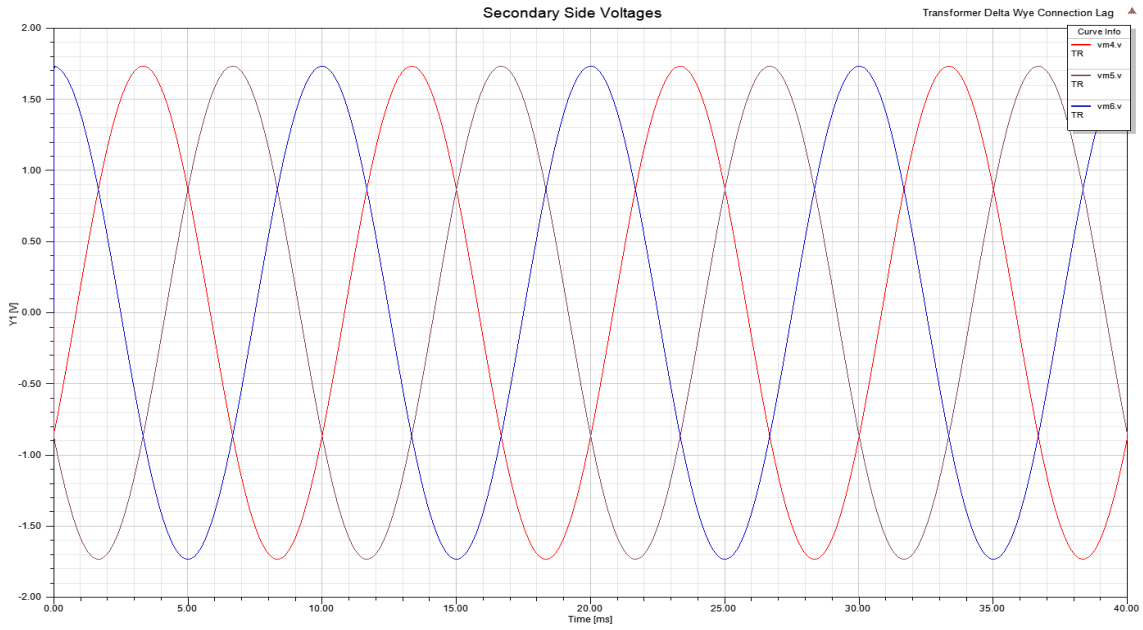


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

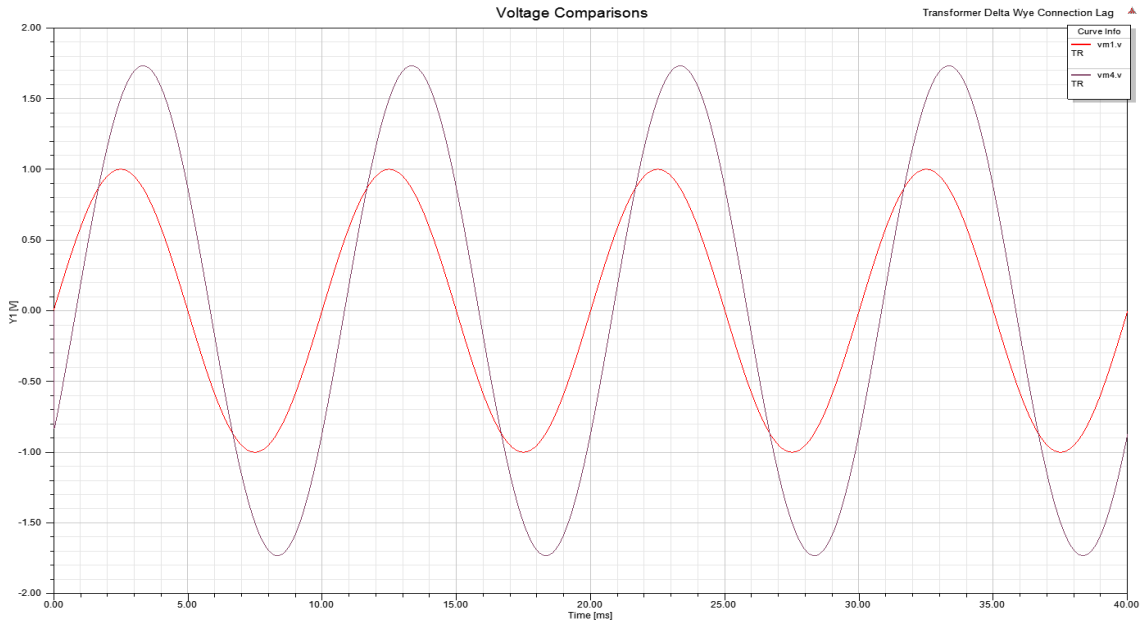


Figure 4: Voltage Comparison

Transformer Delta-Wye Connection Lead Example

Description

The transformer Delta-Wye connection lag schematic is shown in Figure 1.

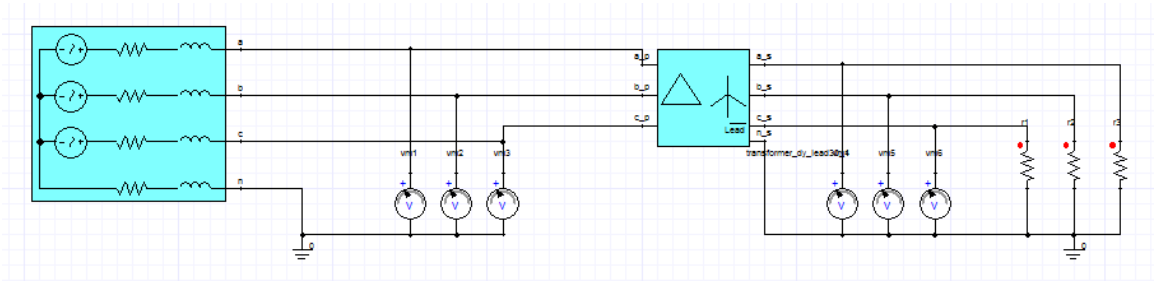


Figure 1: Transformer Delta-Wye Connection Lead Example Schematic

The system contains the transformer_dy_lead30 from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer delta-wye connection lead 30 degree in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

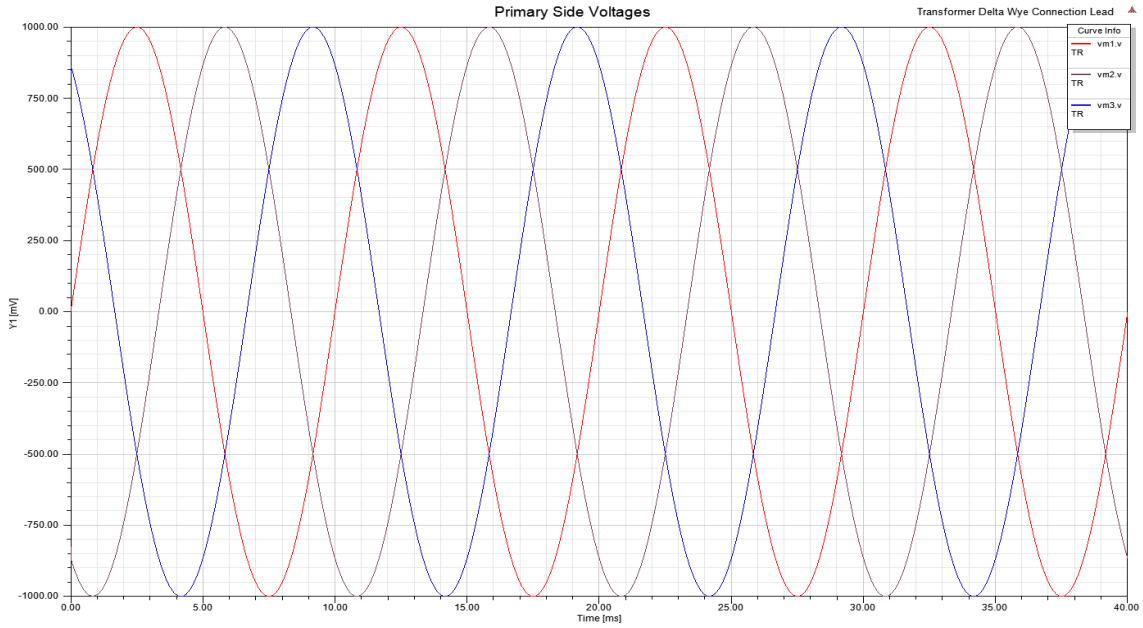


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

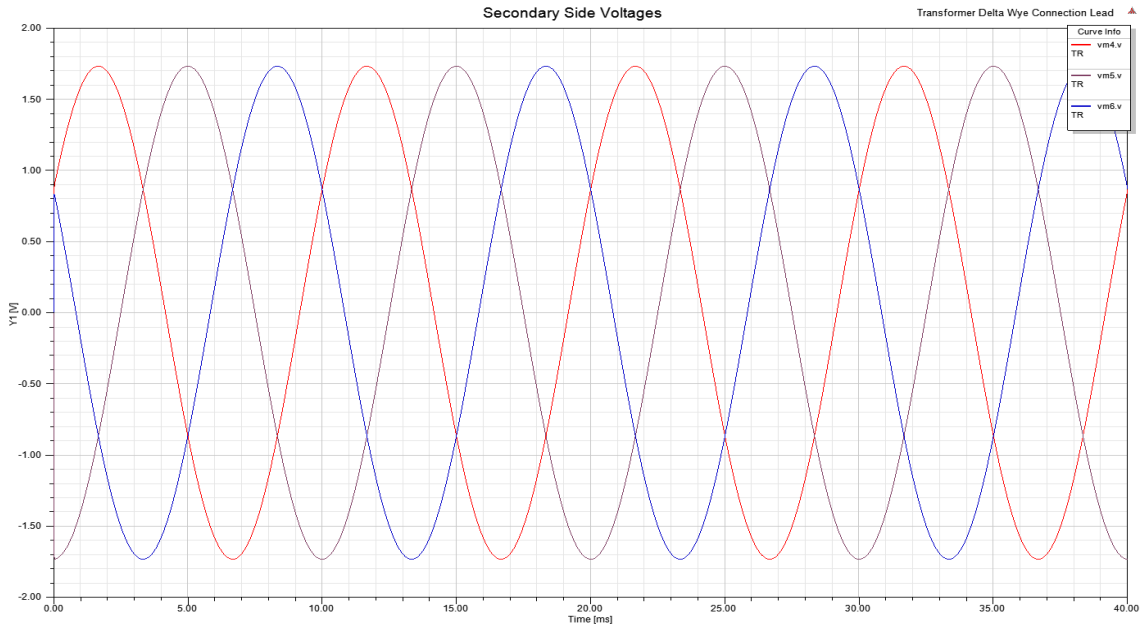


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

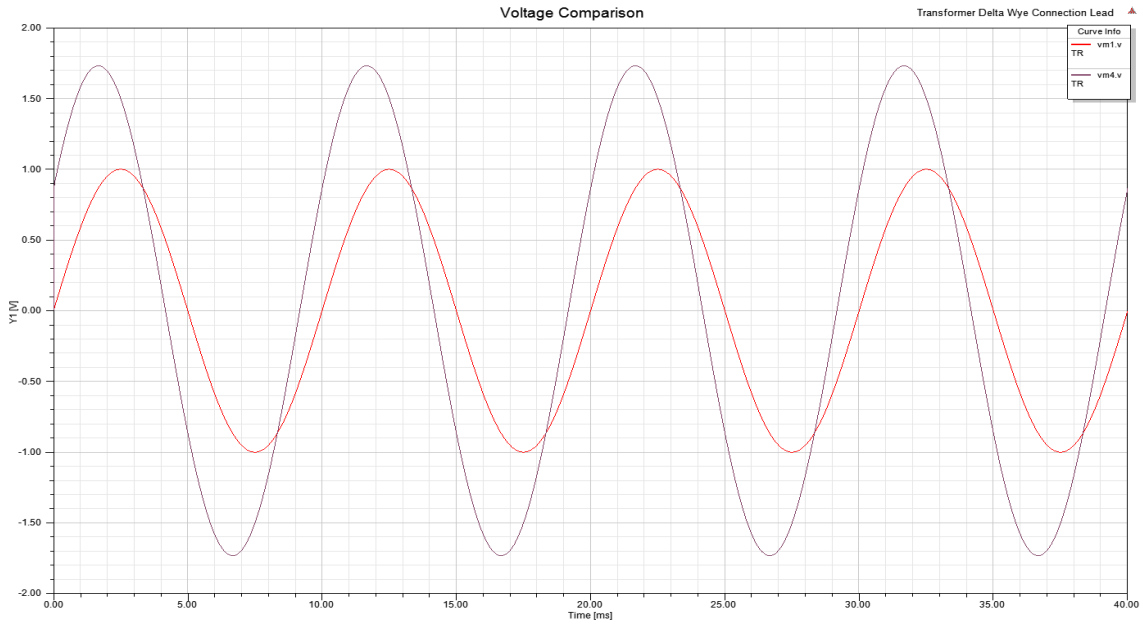


Figure 4: Voltage Comparison

Transformer Wye-Delta Connection Lag Example

Description

The transformer Wye-Delta connection lag schematic is shown in Figure 1.

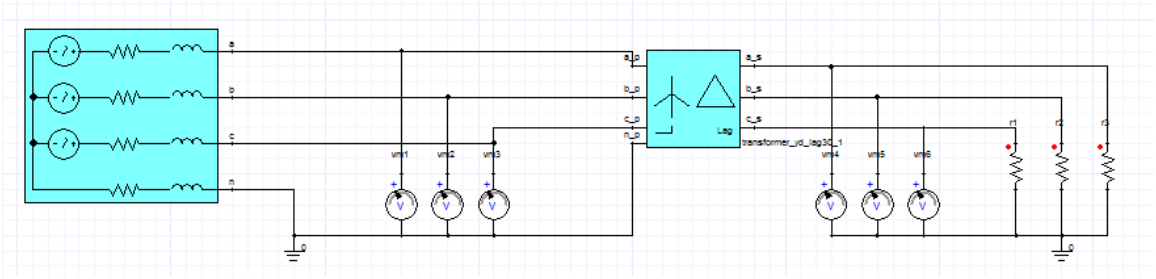


Figure 1: Transformer Wye-Delta Connection Lag Example Schematic

The system contains the transformer_yd_lag30 from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer wye-delta connection lag 30 degree in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

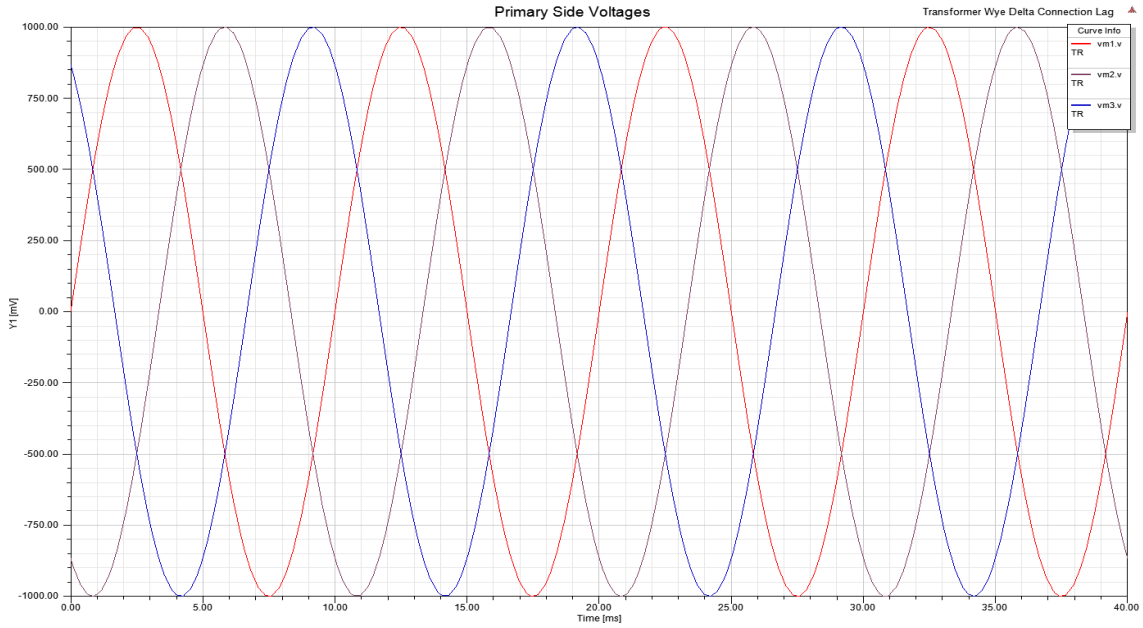


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

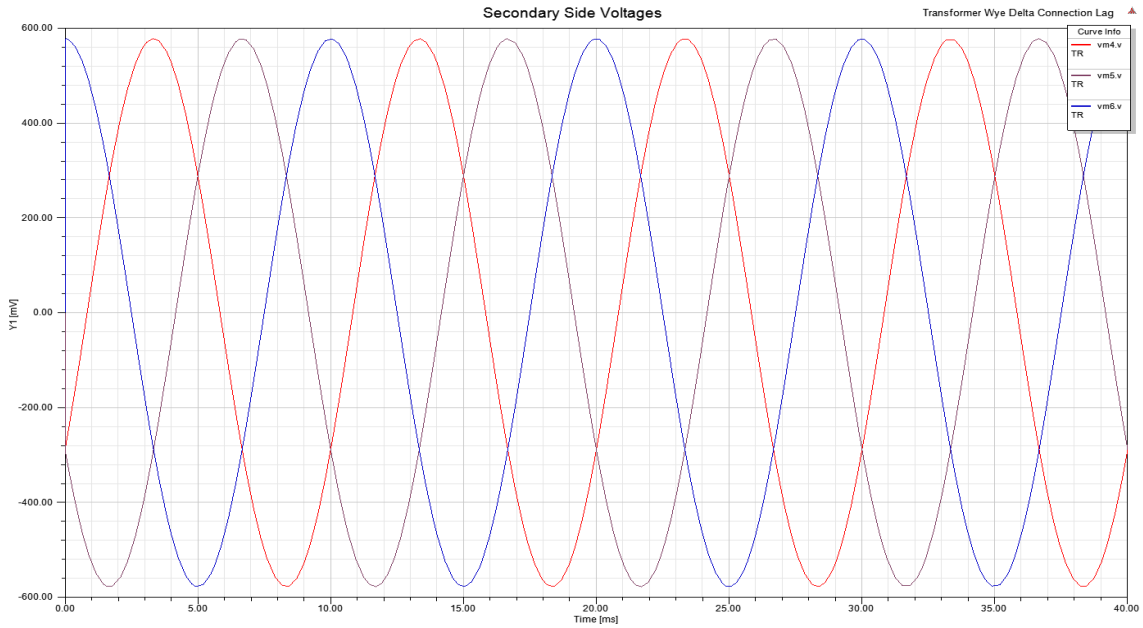


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

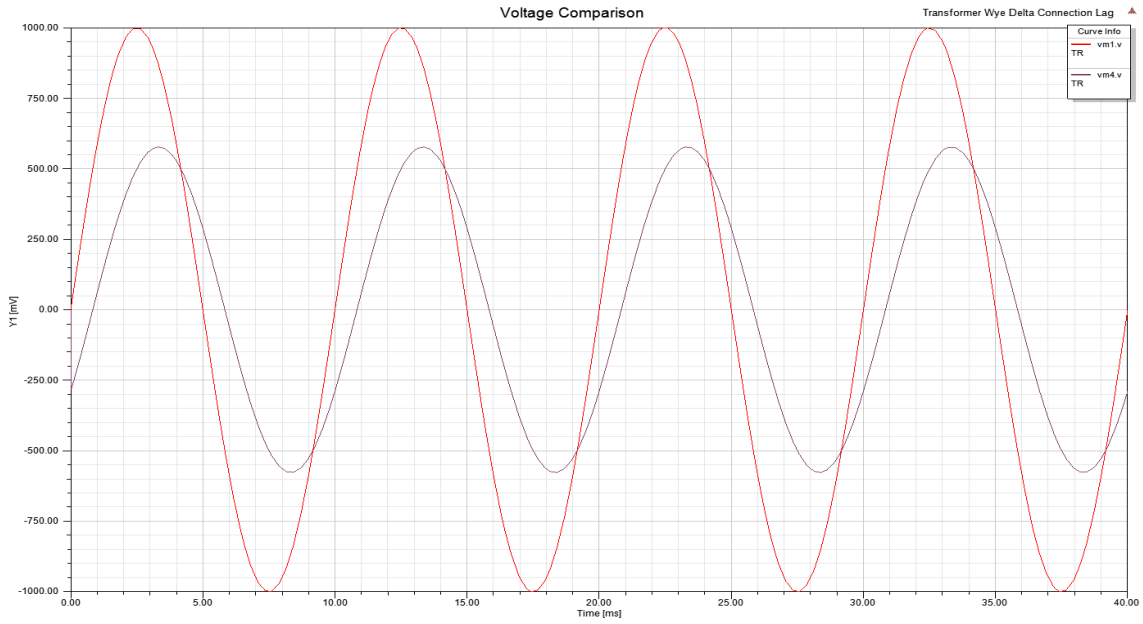


Figure 4: Voltage Comparison

Transformer Wye-Delta Connection Lead Example

Description

The transformer Wye-Delta connection lead schematic is shown in Figure 1.

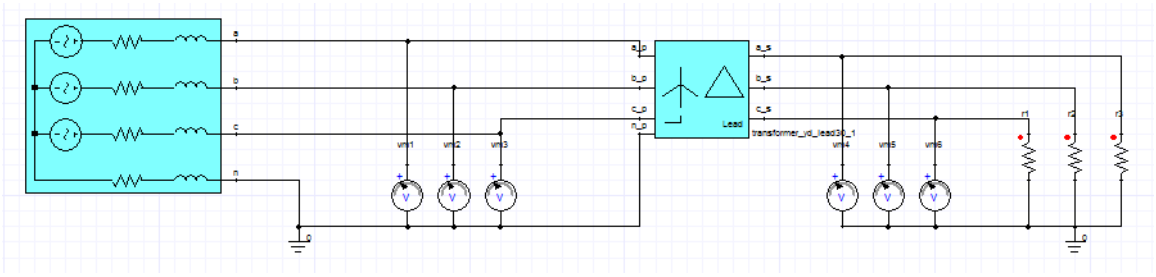


Figure 1: Transformer Wye-Delta Connection Lead Example Schematic

The system contains the transformer_yd_lead30 from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer wye-delta connection lead 30 degree in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

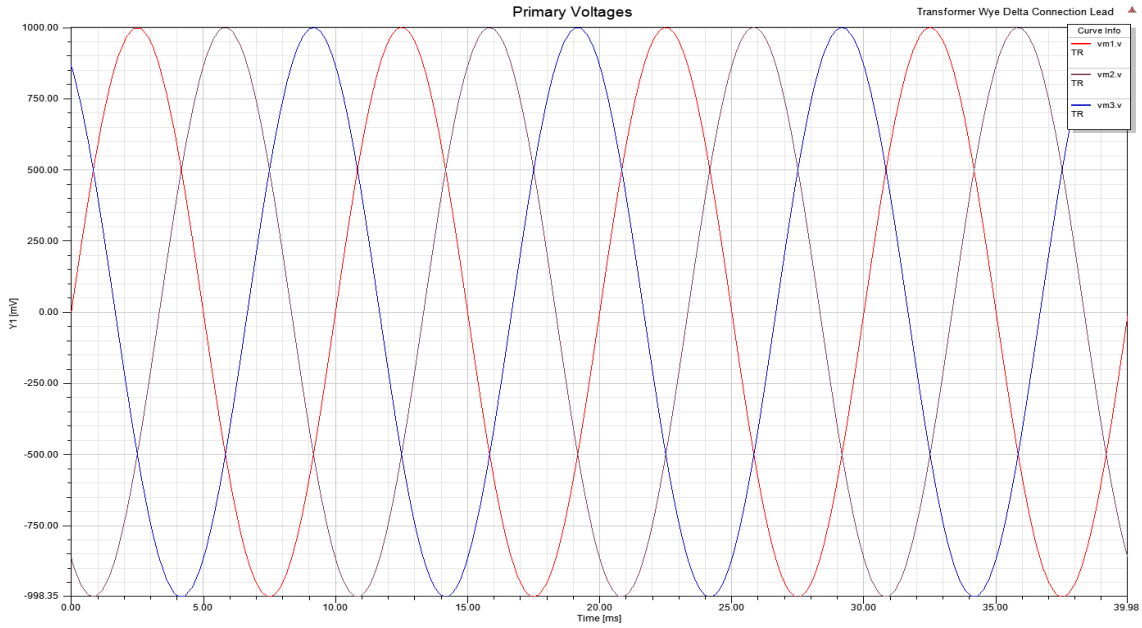


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

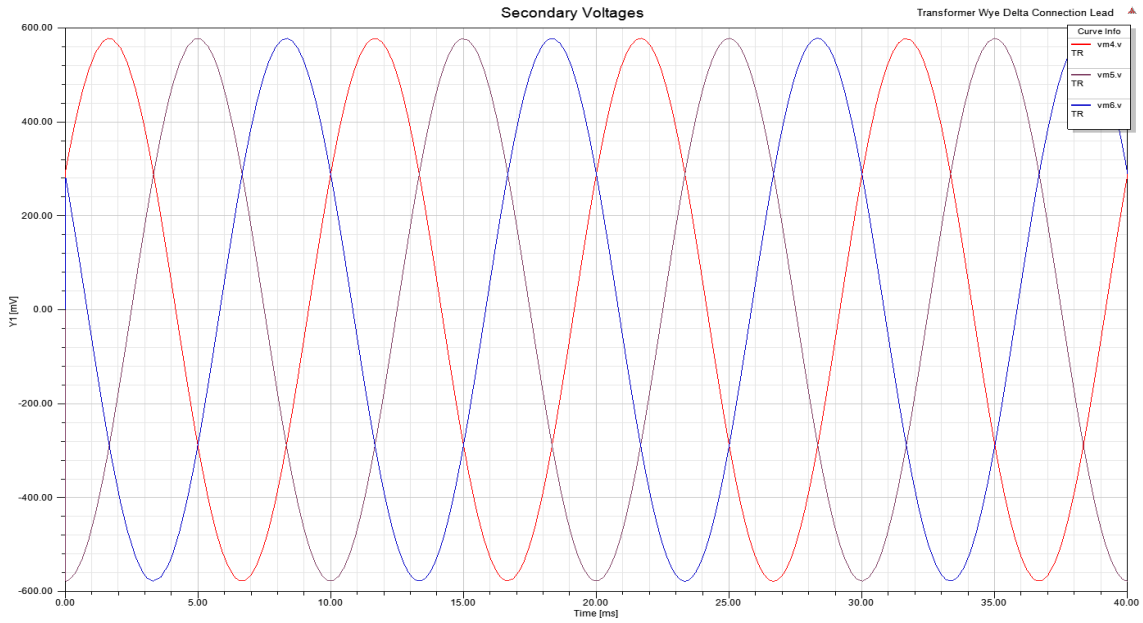


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

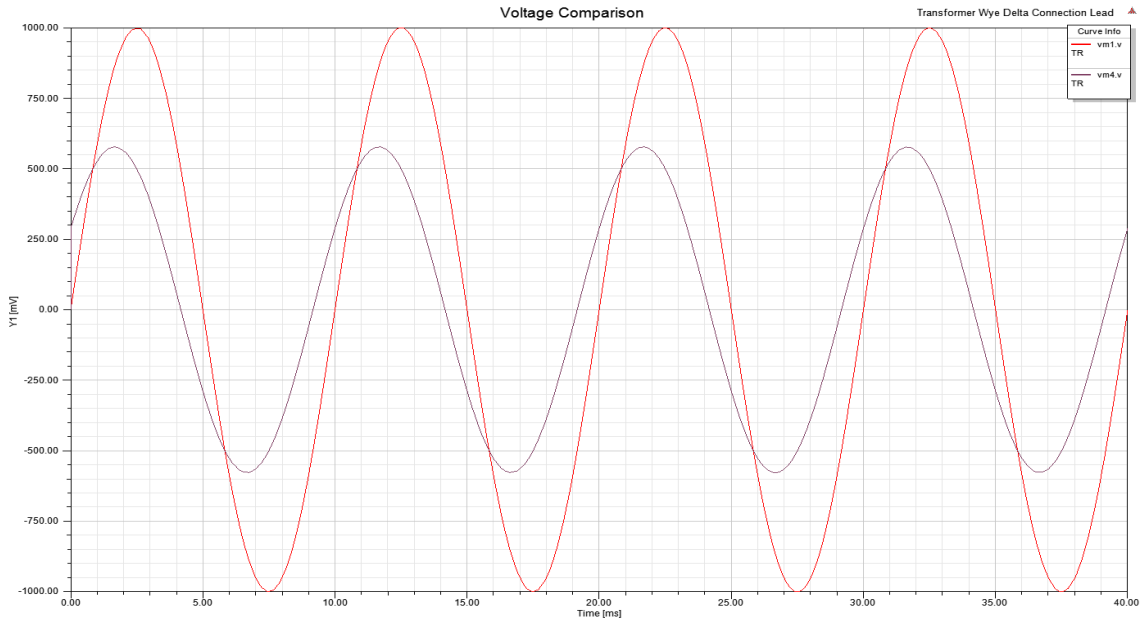


Figure 4: Voltage Comparison

Transformer Wye-Delta-Wye Connection Lag Example

Description

The transformer Wye-Delta-Wye connectionlag schematic is shown in Figure 1.

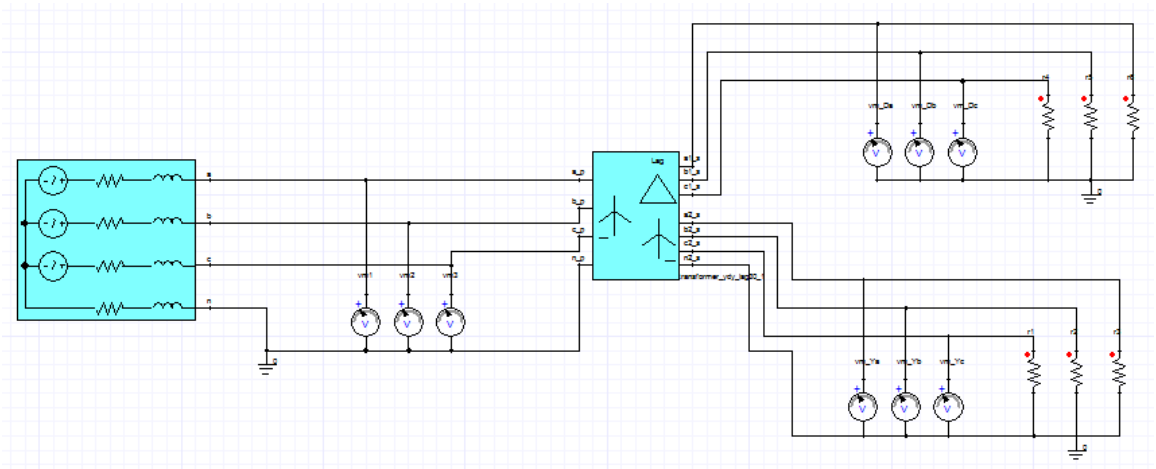


Figure 1: Transformer Wye-Delta-Wye Connection Lag Example Schematic

The system contains the transformer_ydy_lag from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer wye-delta-wye connection lag in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

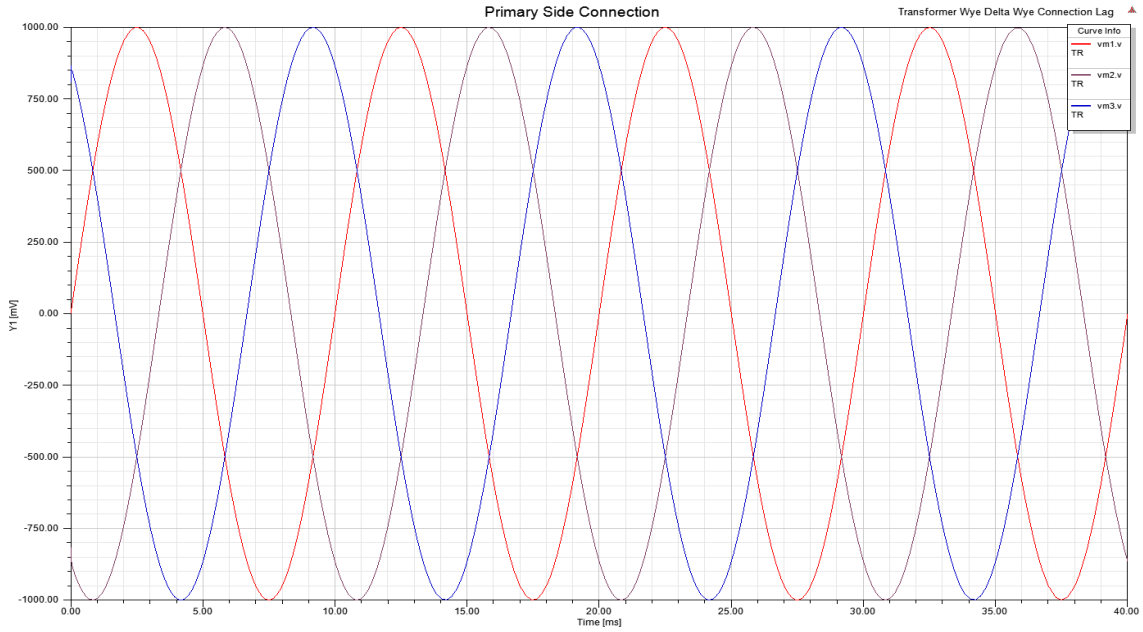


Figure 2: Primary Side Voltages

The secondary side Delta connection voltages are shown in Figure 3.

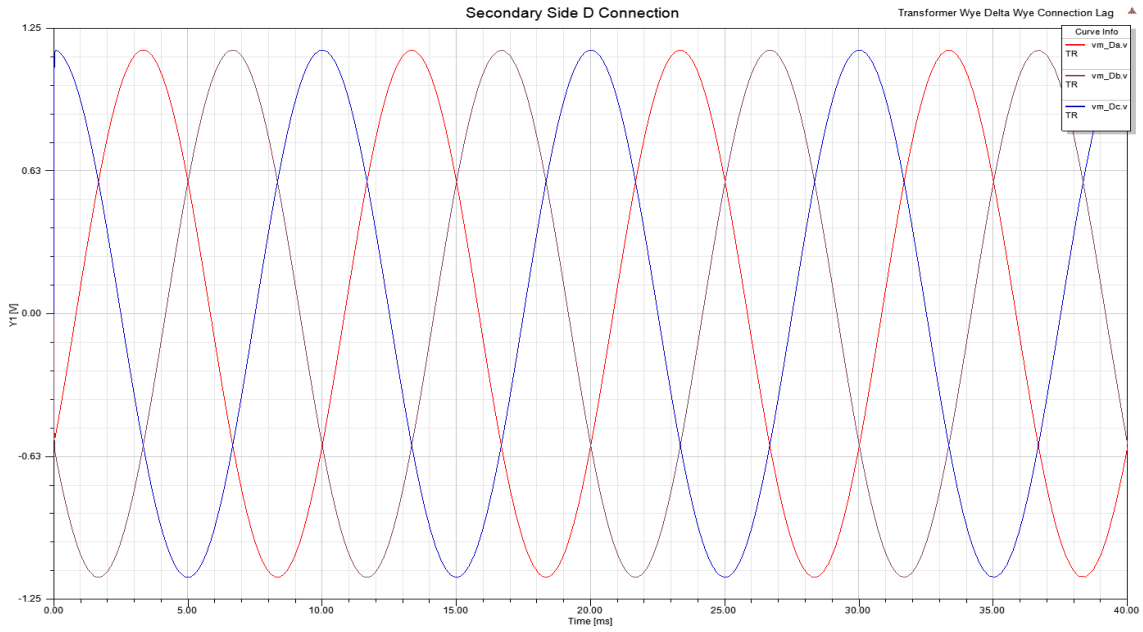


Figure 3: Secondary Side D Voltages

The secondary side Wye connection voltages are shown in Figure 4.

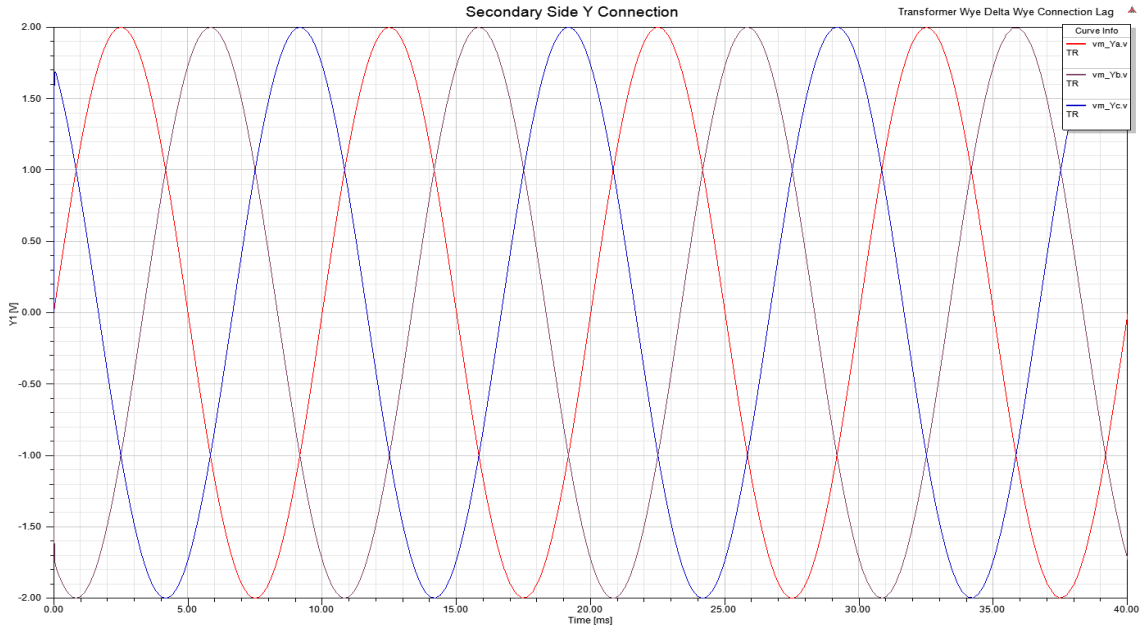


Figure 4: Secondary Side Y Voltages

The voltage comparison are shown in Figure 5.

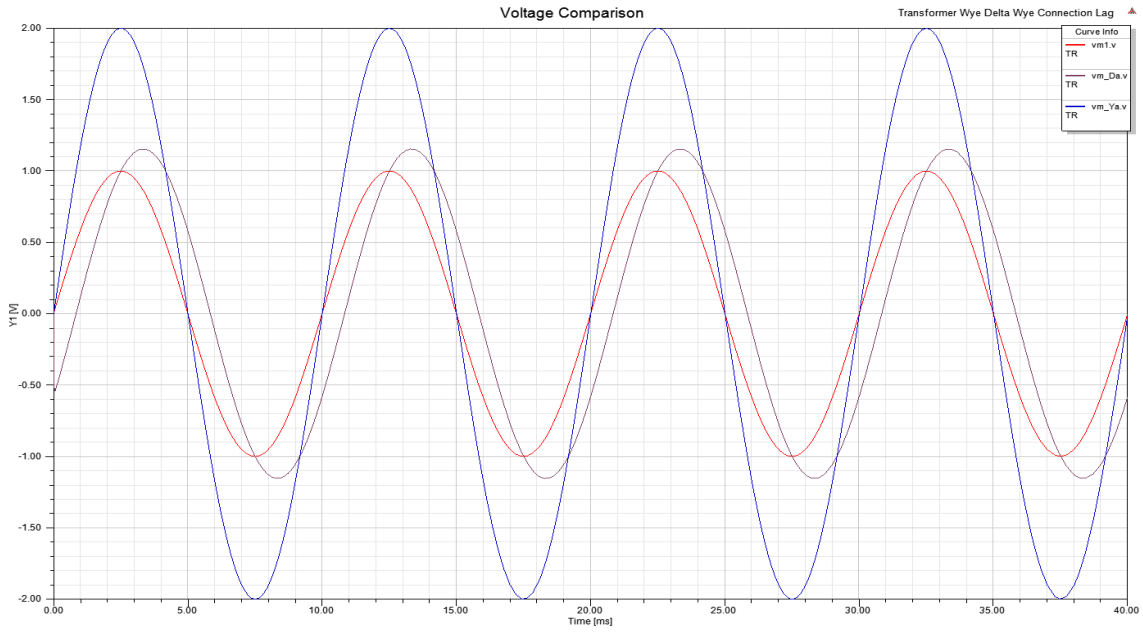


Figure 5: Voltage Comparison

Transformer Wye-Delta-Wye Connection Lead Example

Description

The transformer Wye-Delta-Wye connectionlead schematic is shown in Figure 1.

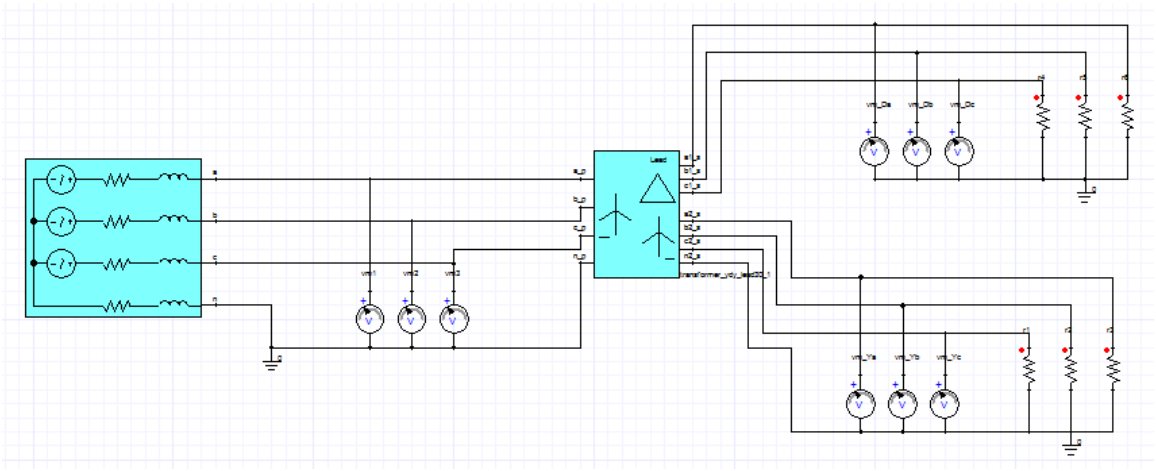


Figure 1: Transformer Wye-Delta-Wye Connection Lead Example Schematic

The system contains the transformer_ydy_lead from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer wye-delta-wye connection lead in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

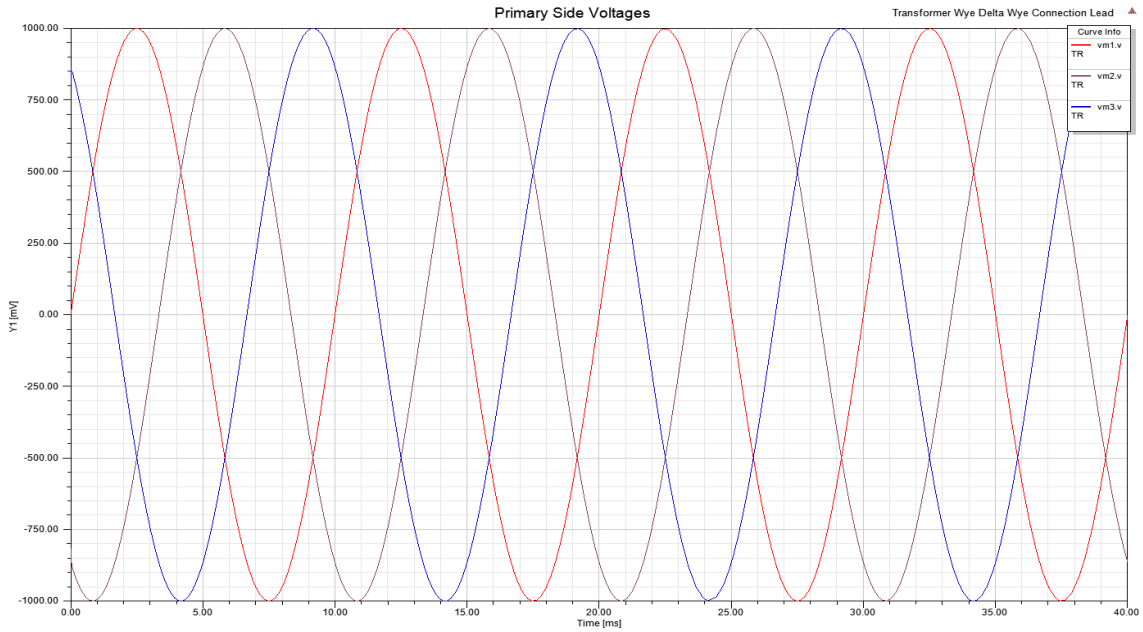


Figure 2: Primary Side Voltages

The secondary side Delta connection voltages are shown in Figure 3.

Figure 3: Secondary Side D Voltages

The secondary side Wye connection voltages are shown in Figure 4.

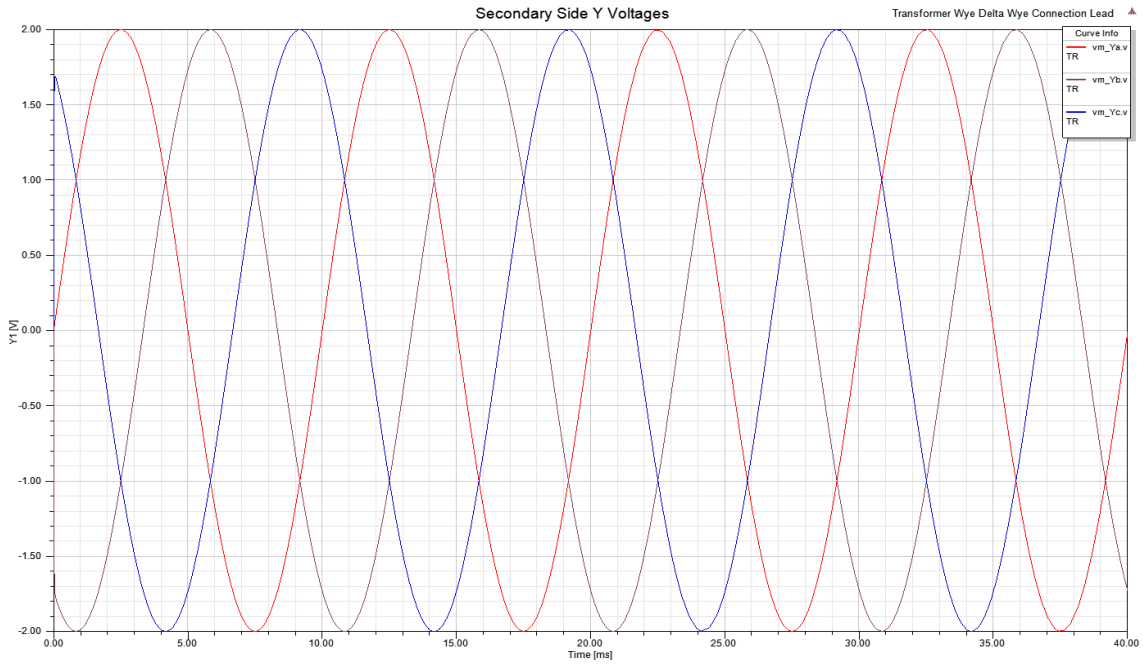


Figure 4: Secondary Side Y Voltages

The voltage comparison are shown in Figure 5.

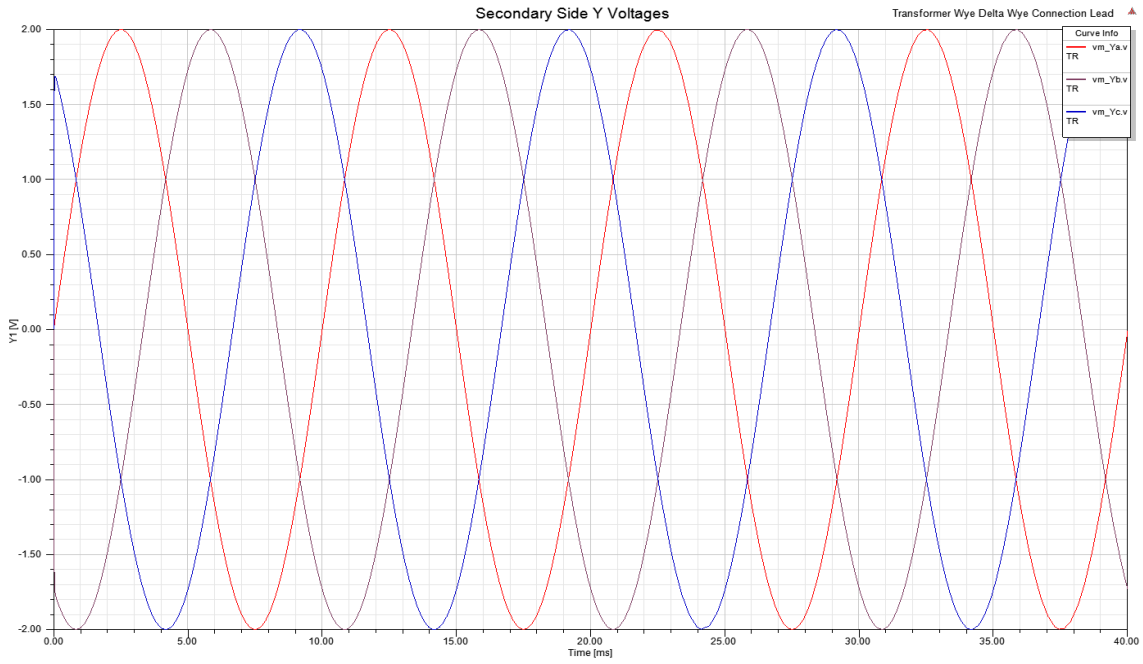


Figure 5: Voltage Comparison

Transformer Wye-Wye Connection Example

Description

The transformer Wye-Wye connection schematic is shown in Figure 1.

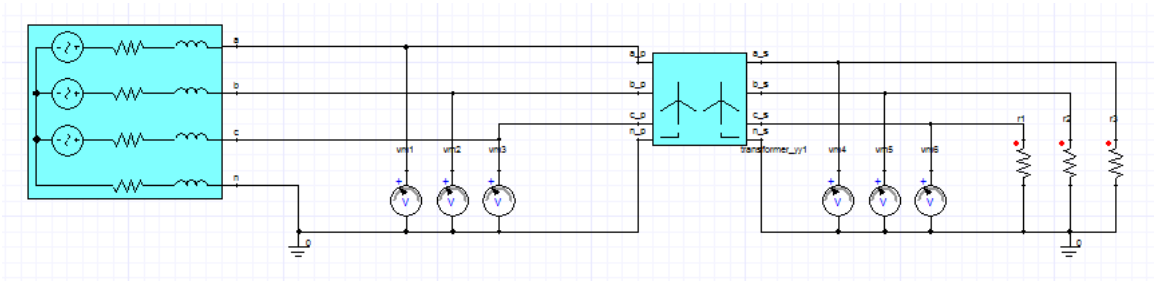


Figure 1: Transformer Wye-Wye Connection Example Schematic

The system contains the transformer_yy from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of transformer wye-wye connection in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The primary side voltages are shown in Figure 2.

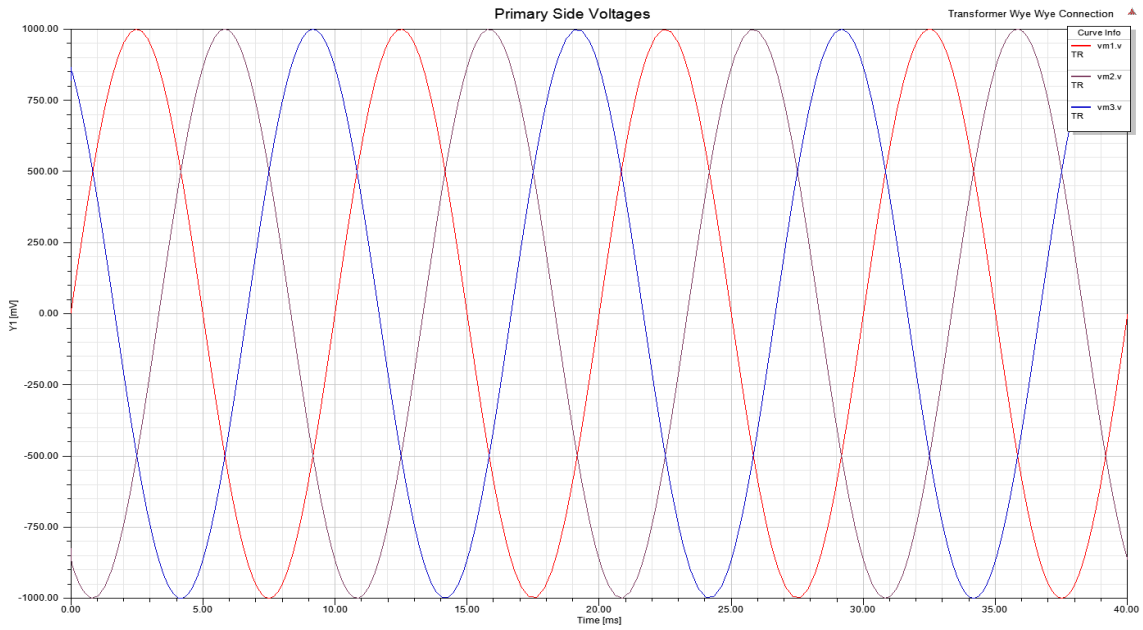


Figure 2: Primary Side Voltages

The secondary side voltages are shown in Figure 3.

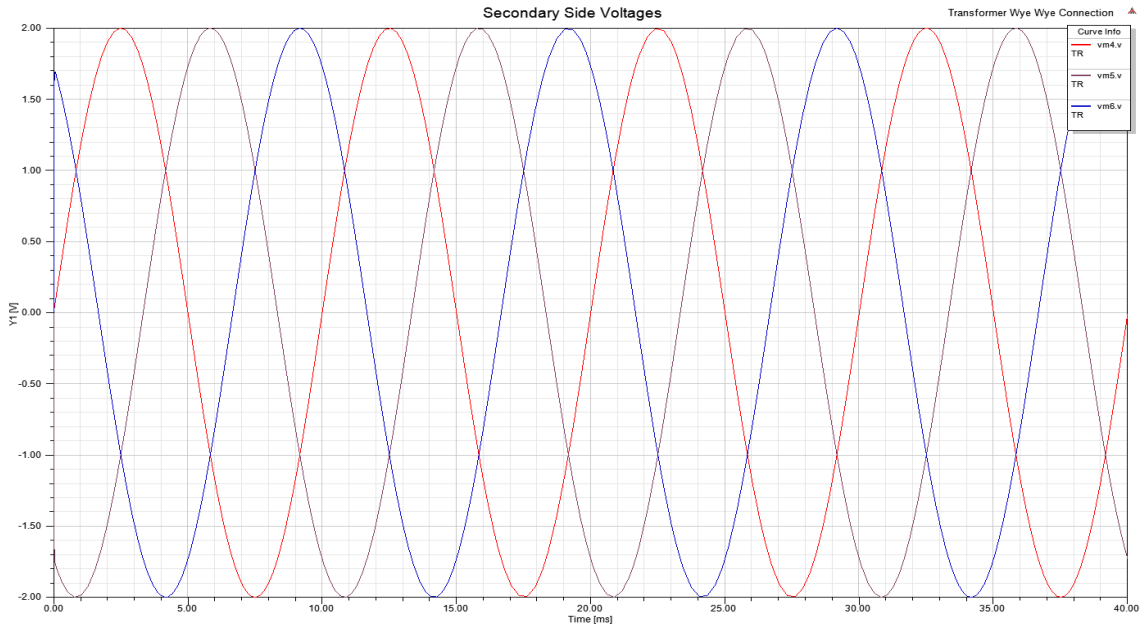


Figure 3: Secondary Side Voltages

The voltage comparison are shown in Figure 4.

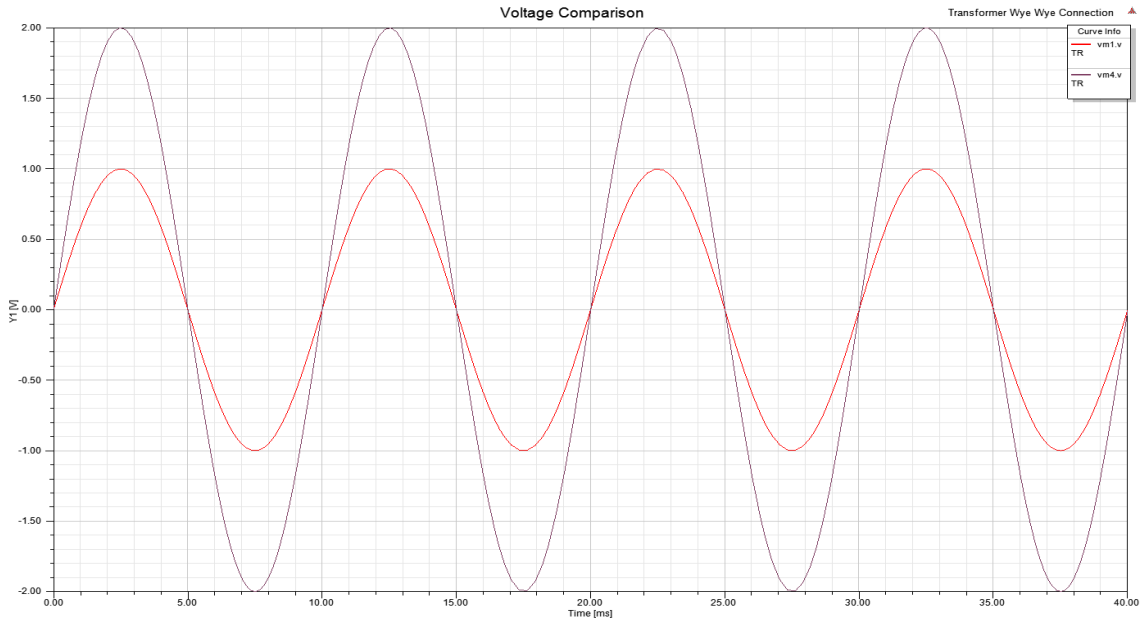


Figure 4: Voltage Comparison

Two Level Four Pulse PWM Example

Description

The two level four pulse PWM schematic is shown in Figure 1.

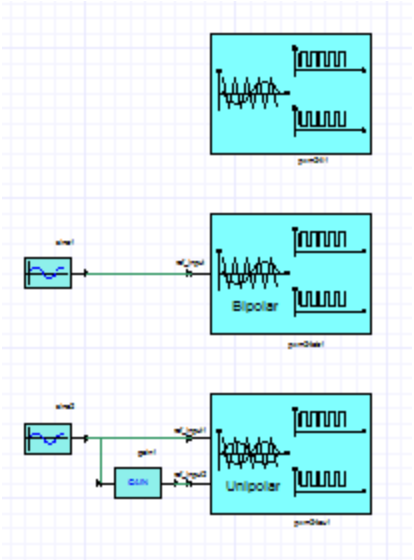


Figure 1: Two Level Four Pulse PWM Schematic

The system contains the pwm24i, pwm24eu and pwm24ebmodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of two level four pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The PWM generator with internal reference signal results are shown in Figure 2.

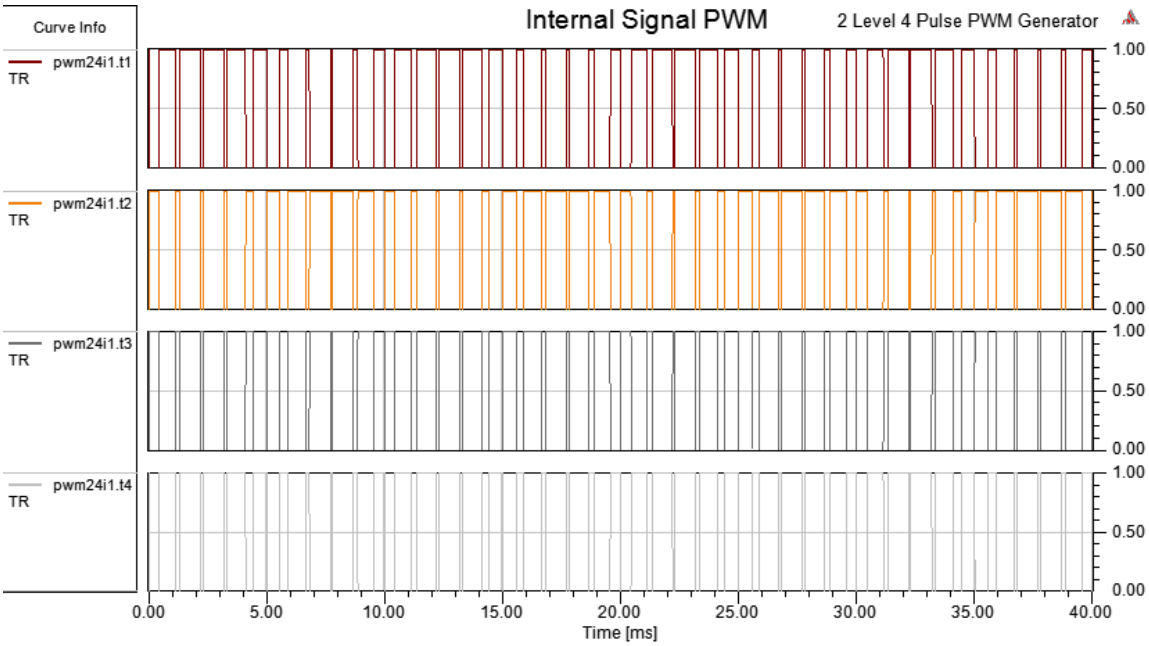


Figure 2: Internal Signal PWM

The PWM generator with external reference signal, unipolar results are shown in Figure 3.

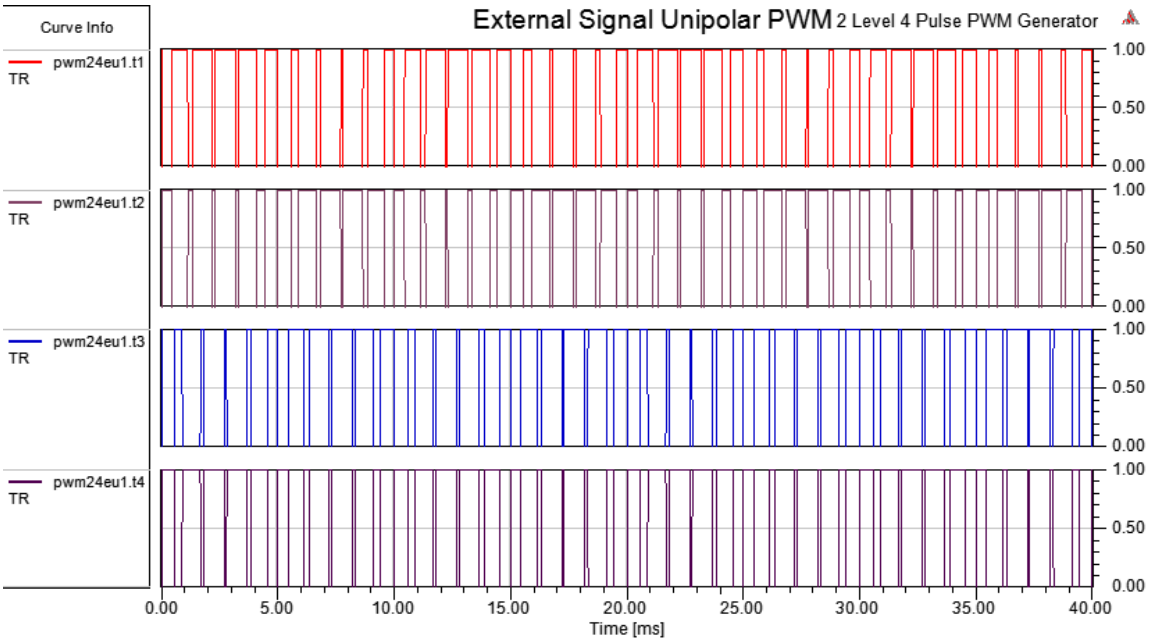


Figure 3: External Signal PWM, Unipolar

The PWM generator with external reference signal, bipolar results are shown in Figure 4.

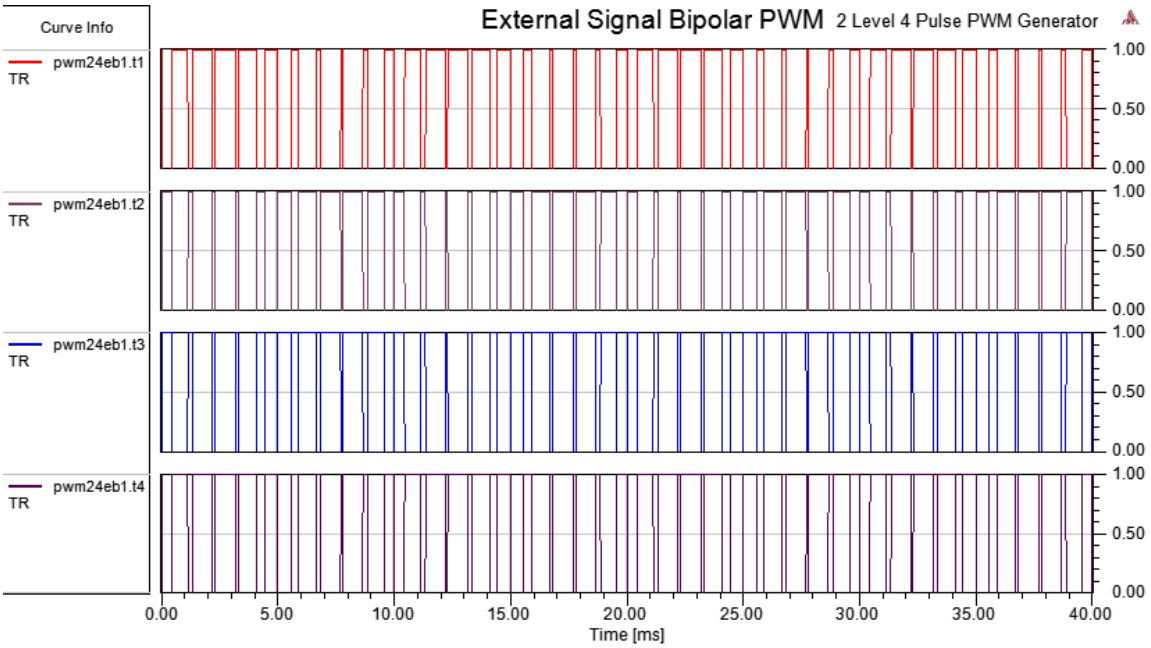


Figure 4: External Signal PWM, Bipolar

Two Level Six Pulse PWM Example

Description

The two level six pulse PWM schematic is shown in Figure 1.

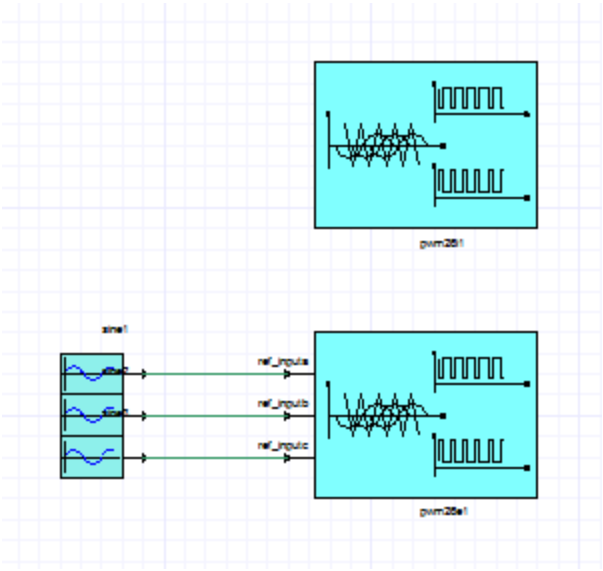


Figure 1: Two Level Six Pulse PWM Schematic

The system contains the pwm26i and pwm26emodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of two level three phase six pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The PWM generator with internal reference signal results are shown in Figure 2.

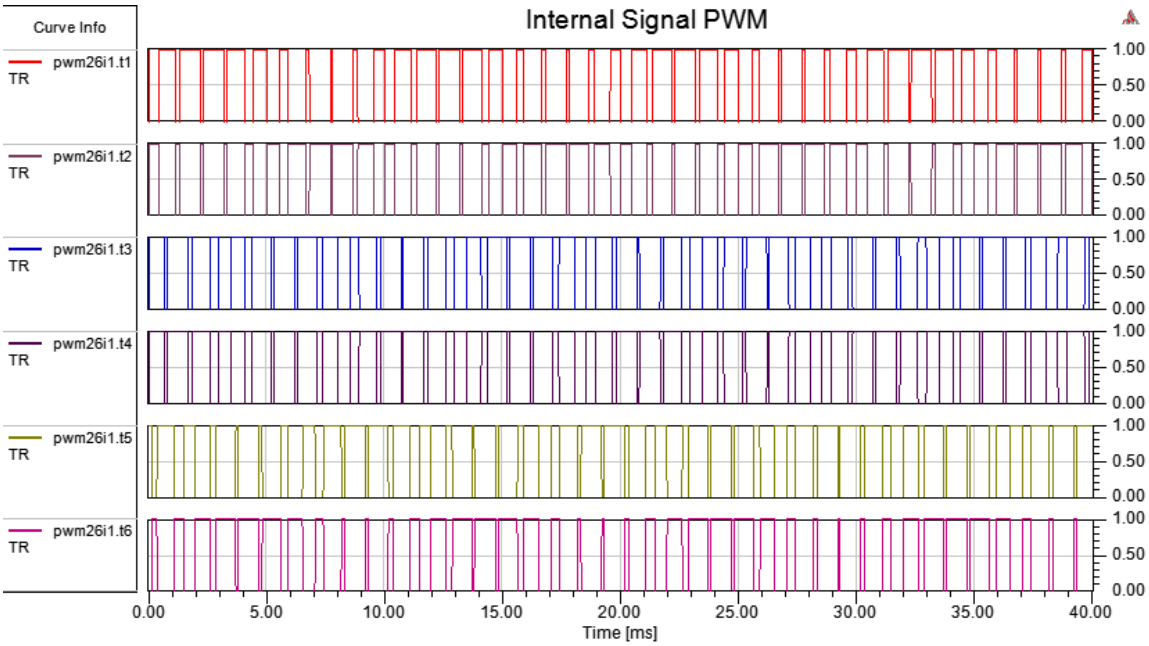


Figure 2: Internal Signal PWM

The PWM generator with external reference signal results are shown in Figure 3.

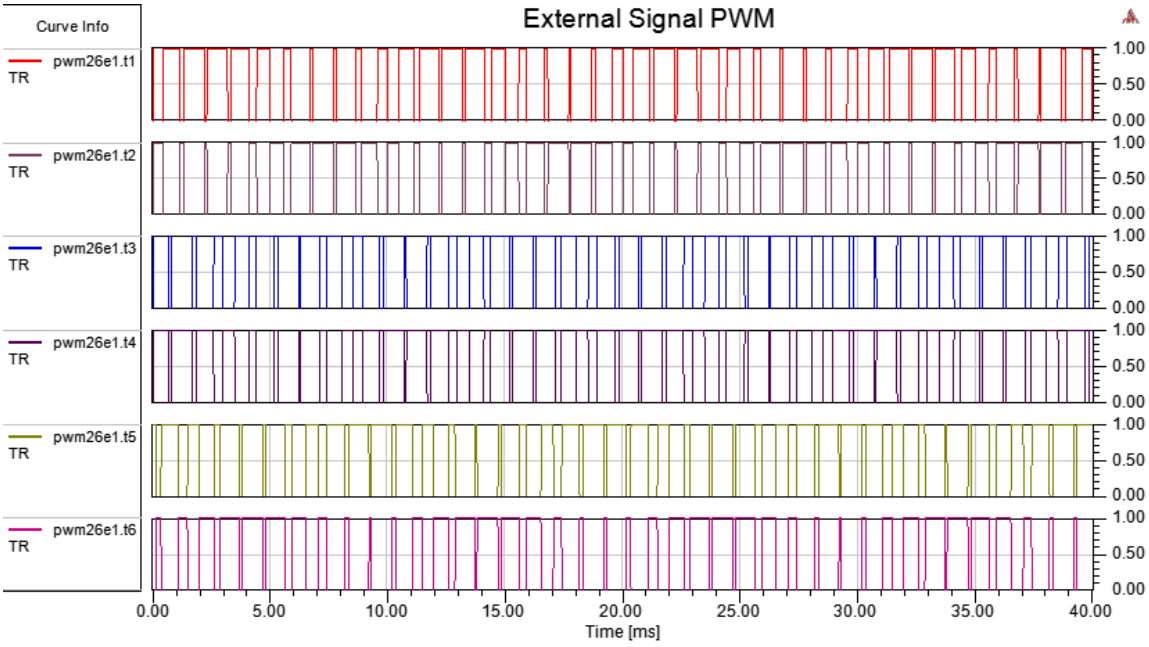


Figure 3: External Signal PWM

Two Level Two Pulse PWM Example

Description

The two level two pulse PWM schematic is shown in Figure 1.

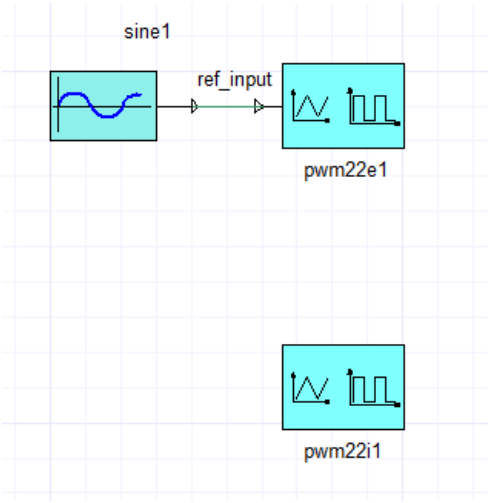


Figure 1: Two Level Two Pulse PWM Schematic

The system contains the pwm22i and pwm22emodels from the Power System VHDL-AMS library.

This example is mainly used for demonstrating the usage of two level two pulse PWM components in the Power System VHDL-AMS library. The results are shown below.

Simulation Results

The control signals are shown in Figure 2.

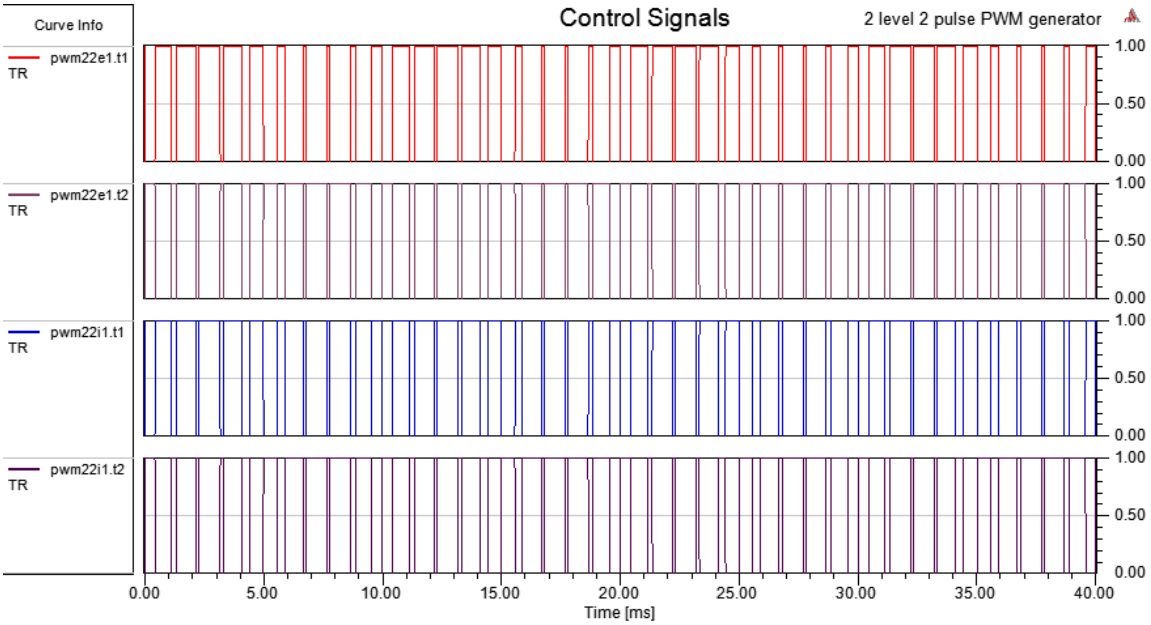


Figure 2: Control Signals